

**OLMS63K SERIES 4-bit Low Power MCU CHECK LIST****Part No.: ML63189C -**

This list is to avoid unnecessary troubles in programming and application circuit. Please confirm if all the points below have been checked and return this list together with customer's software. If there is any question concerning this check list, please feel free to contact us.

**(1) PACKAGE**

Chip Form :  128-pin QFP Form : GA

**(2) VOLTAGE SUPPLY**

When Back up is used ( $V_{DD}=0.9V$  to  $2.7V$ )

Upon reset, the BACKUP bit is set to "1" to enter the back up state.

When Back up is not used ( $V_{DD}=1.8V$  to  $5.5V$ )

To release the back up state, the BACKUP bit should be reset "0".

Connect  $V_{DD}$  to  $V_{DDH}$  externally.

Since  $V_{DDI}$  is separated from the positive power supply pin ( $V_{DD}$ ), power must be supplied to the  $V_{DDI}$  pin.

If a port is to be connected to an external device that operates on a different power supply, the power supply of the external device must be fed to the  $V_{DDI}$  pin.

**(3) OSCILLATION & FREQUENCY**

Low-speed oscillation

When Crystal oscillation is used

Crystal oscillation frequency 32.768k to 76.8kHz ( $V_{DD}=0.9V$  to  $5.5V$ )

When RC oscillation is used

RC oscillation frequency 32k to 80kHz  $\pm$  30% ( $R_{OSL}=1.5M$  to  $500k\Omega$  /  $V_{DD}=0.9V$  to  $5.5V$ )

High-speed oscillation

When ceramic oscillation is used

When backup is used 300k to 500kHz ( $V_{DD}=1.2V$  to  $2.7V$ )

200k to 1MHz ( $V_{DD}=1.5V$  to  $2.7V$ )

When backup is not used

200k to 2MHz ( $V_{DD}=1.8V$  to  $5.5V$ )

When RC oscillation is used

When backup is used 200k to 1MHz  $\pm$  30% ( $R_{OSH}=400k$  to  $75k\Omega$  /  $V_{DD}=1.2V$  to  $2.7V$ )

When backup is not used 700k to 1.35MHz  $\pm$  30% ( $R_{OSH}=100k$  to  $51k\Omega$  /  $V_{DD}=1.8V$  to  $5.5V$ )

2MHz  $\pm$  30% ( $R_{OSH}=30k\Omega$  /  $V_{DD}=1.8V$  to  $3.5V$ )

**(4) BATTERY LOW DETECTION CIRCUIT (BLD)**

Enable BLD only when battery check is carried out.

Read the BLDF flag 1ms or more after setting the ENBL to "1".

Four levels of judgment voltage can be selected by the BLDCON bits.

Judgment voltage values ( $T_a=25$  degree C) :

$1.05 \pm 0.10V$ ,  $1.20 \pm 0.10V$ ,  $1.80 \pm 0.10V$ ,  $2.40 \pm 0.10V$

When verifying BLD operation, the operation must be verified with an evaluation sample device.

[ The development-support tool (EASE63180) do not support BLD function. ]

**(5) HIGH SPEED CLOCK OSCILLATION CIRCUIT**

- RC Oscillation Mode (OSCSEL=0)  
T<sub>WAIT</sub>=300μs or longer after ENOSC=1
- Ceramic Oscillation Mode (OSCSEL=1)  
T<sub>WAIT</sub>=10ms or longer after ENOSC=1
- When changing the High-speed clock to Low-speed one, reset CPUCLK to "0" first and after that reset ENOSC to "0". Never reset both at the same time, and follow the above turn.

**(6) USABLE ROM SIZE**

- 32736 × 16 bits

**(7) USABLE STACK SIZE**

- Call stack : 16 levels
- Register stack : 16 levels

**(8) INITIALIZATION OF RAM**

- RAM content is undefined after power up - remember to do initialization.

**(9) INITIALIZATION OF DISPLAY REGISTER**

- Display Register content is undefined after power up - remember to do initialization.

**(10) LCD DRIVER**

- When the LCD driver is not used, select the power down mode ( PDWN=1 )  
V<sub>DD2</sub> : To connect 0.1μF capacitance between V<sub>DD2</sub> and V<sub>SS</sub> level.  
V<sub>DD1</sub>, V<sub>DD3</sub>, V<sub>DD4</sub>, V<sub>DD5</sub>, C1, C2 : Open
- BIAS selection
  - 1/5 bias
  - 1/4 bias
- To connect V<sub>DD3</sub> to V<sub>DD2</sub>.

**(11) INPUT PORTS AND I/O PORTS**

- When selecting High impedance input, the port should be connected to V<sub>DD</sub> or V<sub>SS</sub>.

**(12) MASK OPTION**

- The ML63189C can select the crystal oscillation circuit or the RC oscillation circuit for the low-speed clock oscillation circuit by mask option.  
To use the mask option, assign mask option data in the application program in accordance with the format below.

Address	Data	
7FE0H	0 : Crystal oscillation	: RC oscillation

**(13) RESET SAMPLING CIRCUIT**

- The ML63189C has a RESET Sampling Circuit.  
When performing transfer to the system reset mode by setting the RESET pin to a "H" level, set the RESET pulse width to 1 ms or more.

**(14) MELODY DRIVER**

[ ] When terminating melody playing forcibly, software have to comply with the following description.

; \*\*\* Program part \*\*\*

```

DI                ; (1) Disable master interrupt.
MSA    MDSTOP_DATA ; (2) Write melody end data to the melody circuit.
MOV     A, #0      ; (3) Set the MSF flag to "0".
MOV     MDCON, A
MOV     A, #1101b  ; (4) Clear melody interrupt request (QMD)
AND     IRA0, A    ; (5) Enable master interrupt(MIE)
EI

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; \*\*\* ROM table data part \*\*\*

; \*\*\* Provide two items of melody data so that a melody will always be terminated  
; \*\*\* even if a melody request is issued twice.

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MDSTOP_DATA:
DW     8000H      ; Silence data 1
DW     8000H      ; Silence data 2
;*****

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We, \_\_\_\_\_, hereby confirm that all the points stated above have been checked.

\_\_\_\_\_  
Signature

\_\_\_\_\_  
Date