

OLMS63K SERIES 4-bit Low Power MCU CHECK LIST**Part No.: MSM63184B -**

This list is to avoid unnecessary troubles in programming and application circuit. Please confirm if all the points below have been checked and return this list together with customer's software. If there is any question concerning this check list, please feel free to contact us.

(1) PACKAGE

Chip Form : 128-pin QFP Form : GS-K

(2) VOLTAGE SUPPLY

When Back up is used ($V_{DD}=0.9V$ to $2.7V$)

Upon reset, the BACKUP bit is set to "1" to enter the back up state.

When Back up is not used ($V_{DD}=1.8V$ to $5.5V$)

To release the back up state, the BACKUP bit should be reset "0".

Connect V_{DD} to V_{DDH} externally.

Since V_{DDI} is separated from the positive power supply pin (V_{DD}), power must be supplied to the V_{DDI} pin.

If a port is to be connected to an external device that operates on a different power supply, the power supply of the external device must be fed to the V_{DDI} pin.

(3) OSCILLATION & FREQUENCY

Low-speed oscillation

Crystal oscillation frequency 30k to 35kHz ($V_{DD}=0.9V$ to $5.5V$)

High-speed oscillation

When ceramic oscillation is used

When backup is used 300k to 500kHz ($V_{DD}=1.2V$ to $2.7V$)

200k to 1MHz ($V_{DD}=1.5V$ to $2.7V$)

When backup is not used 300k to 500kHz ($V_{DD}=1.8V$ to $5.5V$)

300k to 1MHz ($V_{DD}=2.2V$ to $5.5V$)

200k to 2MHz ($V_{DD}=2.7V$ to $5.5V$)

When RC oscillation is used

When backup is used 100k to 300k Ω ($V_{DD}=1.2V$ to $2.7V$)

50k to 300k Ω ($V_{DD}=1.5V$ to $2.7V$)

When backup is not used 100k to 300k Ω ($V_{DD}=1.8V$ to $5.5V$)

50k to 300k Ω ($V_{DD}=2.2V$ to $5.5V$)

30k to 300k Ω ($V_{DD}=2.7V$ to $5.5V$)

(4) BATTERY LOW DETECTION CIRCUIT (BLD)

Enable BLD only when battery check is carried out.

Read the BLDF flag 10ms or more after setting the ENBL to "1".

Four levels of judgment voltage can be selected by the BLDCON bits.

Judgment voltage values :

$1.05 \pm 0.10V$, $1.30 \pm 0.15V$, $2.20 \pm 0.20V$, $2.80 \pm 0.30V$

(5) HIGH SPEED CLOCK OSCILLATION CIRCUIT

- RC Oscillation Mode (OSCSEL=0)
T_{WAIT}=6ms or longer after ENOSC=1
- Ceramic Oscillation Mode (OSCSEL=1)
T_{WAIT}=10ms or longer after ENOSC=1
- When changing the High-speed clock to Low-speed one, reset CPUCLK to "0" first and after that reset ENOSC to "0". Never reset both at the same time, and follow the above turn.

(6) USABLE ROM SIZE

- 8160 × 16 bits

(7) USABLE STACK SIZE

- Call stack : 8 levels
- Register stack : 16 levels

(8) INITIALIZATION OF RAM

- RAM content is undefined after power up - remember to do initialization.

(9) INITIALIZATION OF DISPLAY REGISTER

- Display Register content is undefined after power up - remember to do initialization.

(10) LCD DRIVER

- When the LCD driver is not used, select the power down mode (PDWN=1)
V_{DD2} : To connect 0.1μF capacitance between V_{DD2} and V_{SS} level.
V_{DD1}, V_{DD3}, V_{DD4}, V_{DD5}, C1, C2 : Open
- BIAS selection
 - 1/5 bias
 - 1/4 bias
 To connect V_{DD3} to V_{DD2}.

(11) INPUT PORTS AND I/O PORTS

- When selecting High impedance input, the port should be connected to "V_{DD}" or "V_{SS}".

We, _____, hereby confirm that all the points stated above have been checked.

Signature

Data