

OLMS63K SERIES 4-bit Low Power MCU CHECK LIST

Part No.: ML63193-

The function of this form is just for reminding the customer to (i) avoid commonly-made programming mistakes and, (ii) notice frequently overlooked or misunderstood hardware features of the caption MCU. The customer is required to fill in this form and submit it with all the other necessary files and documents when the code is released. The actual masking of the MCU is based on the code released by the customer - it is NOT based on the information given in this form. OKI and her distributors are not held liable for any discrepancies between the released code and the information given below.

(1) PACKAGE

Chip Form : 144-pin LQFP Form : TC

(2) VOLTAGE SUPPLY

- When Back up is used ($V_{DD}=0.9V$ to $2.7V$)
Upon reset, the BACKUP bit is set to "1" to enter the back up state.
- When Back up is not used ($V_{DD}=1.8V$ to $5.5V$)
To release the back up state, the BACKUP bit should be reset "0".
Connect V_{DD} to V_{DDH} externally.
- Since V_{DDI} is separated from the positive power supply pin (V_{DD}), power must be supplied to the V_{DDI} pin.
If a port is to be connected to an external device that operates on a different power supply, the power supply of the external device must be fed to the V_{DDI} pin.

(3) OSCILLATION & FREQUENCY

Low-speed oscillation

- When Crystal oscillation is used
Crystal oscillation frequency 32.768k to 76.8kHz ($V_{DD}=0.9V$ to $5.5V$)
- When RC oscillation is used
RC oscillation frequency 32k to 80kHz $\pm 30\%$ ($R_{OSL}=1.5M$ to $500k\Omega$ / $V_{DD}=0.9V$ to $5.5V$)

High-speed oscillation

- When ceramic oscillation is used
 - When backup is used 300k to 500kHz ($V_{DD}=1.2V$ to $2.7V$)
200k to 1MHz ($V_{DD}=1.5V$ to $2.7V$)
 - When backup is not used 200k to 2MHz ($V_{DD}=1.8V$ to $5.5V$)
- When RC oscillation is used
 - When backup is used 200k to 1MHz $\pm 30\%$ ($R_{OSH}=400k$ to $75k\Omega$ / $V_{DD}=1.2V$ to $2.7V$)
 - When backup is not used 700k to 1.35MHz $\pm 30\%$ ($R_{OSH}=100k$ to $51k\Omega$ / $V_{DD}=1.8V$ to $5.5V$)
2MHz $\pm 30\%$ ($R_{OSH}=30k\Omega$ / $V_{DD}=1.8V$ to $3.5V$)

(4) BATTERY LOW DETECTION CIRCUIT (BLD)

- Enable BLD only when battery check is carried out.
- Read the BLDF flag 1ms or more after setting the ENBL to "1".
- Four levels of judgment voltage can be selected by the BLDCON bits.
Judgment voltage values ($T_a=25$ degree C) :
1.05 \pm 0.10V, 1.20 \pm 0.10V, 1.80 \pm 0.10V, 2.40 \pm 0.10V
- When verifying BLD operation, the operation must be verified with an evaluation sample device.
 The development-support tool (EASE63180) do not support BLD function.]

(5) HIGH SPEED CLOCK OSCILLATION CIRCUIT

- RC Oscillation Mode (OSCSEL=0)
T_{WAIT}=300μs or longer after ENOSC=1
- Ceramic Oscillation Mode (OSCSEL=1)
T_{WAIT}=10ms or longer after ENOSC=1
- When changing the High-speed clock to Low-speed one, reset CPUCLK to "0" first and after that reset ENOSC to "0". Never reset both at the same time, and follow the above turn.

(6) USABLE ROM SIZE

- 65504 × 16 bits

(7) USABLE STACK SIZE

- Call stack : 16 levels
- Register stack : 16 levels

(8) INITIALIZATION OF RAM

- RAM content is undefined after power up - remember to do initialization.

(9) INITIALIZATION OF DISPLAY REGISTER

- Display Register content is undefined after power up - remember to do initialization.

(10) LCD DRIVER

- When the LCD driver is not used, select the power down mode (PDWN=1)

V_{DD2} : To connect 0.1μF capacitance between V_{DD2} and V_{SS} level.

V_{DD1}, V_{DD3}, V_{DD4}, V_{DD5}, C1, C2 : Open

BIAS selection

- 1/5 bias

- 1/4 bias

To connect V_{DD3} to V_{DD2}.

(11) INPUT PORTS AND I/O PORTS

- When selecting High impedance input, the port should be connected to "V_{DD}" or "V_{SS}".

(12) MELODY DRIVER

- When terminating melody playing forcibly, software have to comply with the following description.

; *** Program part ***

```
DI ; (1) Disable master interrupt.
MSA MDSTOP_DATA ; (2) Write melody end data to the melody circuit.
MOV A, #0 ; (3) Set the MSF flag to "0".
MOV MDCON, A
MOV A, #1101b ; (4) Clear melody interrupt request (QMD)
AND IRA0, A ; (5) Enable master interrupt(MIE)
EI
```

; *** ROM table data part ***

; *** Provide two items of melody data so that a melody will always be terminated
; *** even if a melody request is issued twice.

MDSTOP_DATA:

```
DW 8000H ; Silence data 1
DW 8000H ; Silence data 2
```

(13) MASK OPTION

The ML63193 uses the mask option to specify the following functions:

- Low-speed clock oscillation circuit

Specify the crystal oscillation circuit or the RC oscillation circuit for the low-speed clock oscillation circuit.

Crystal oscillation circuit RC oscillation circuit

- Reset signal sampling

Specify whether or not the reset signal will be sampled at 2 kHz. When specifying “will carry out 2 kHz sampling”, hold the RESET pin at a “H” level for 1 ms or more.

Will carry out 2 kHz sampling Will not carry out 2 kHz sampling

To use the mask option, assign mask option data in the application program in accordance with the formats below.

The mask option area for the device is an application program execution disabled area.

The mask option is set with the two bits (bits 0 and 1) addressed in the mask option area that is assigned to each model.

Function	Mask option area	bit	data	Option to be selected
Low-speed clock oscillation circuit (crystal oscillation / RC oscillation circuit)	FFE0H	bit0	0	<input type="checkbox"/> Crystal oscillation circuit
			1	<input type="checkbox"/> RC oscillation circuit
Reset signal sampling (will / will not carry out 2 kHz sampling)		bit1	0	<input type="checkbox"/> Will carry out 2 kHz sampling
			1	<input type="checkbox"/> Will not carry out 2 kHz sampling

Example of mask option data generation

- When the crystal oscillation circuit is specified for the low-speed clock oscillation circuit and not carrying out reset signal sampling is specified in the ML63193.

ORG FFE0H ; Use an assembler pseudo-instruction to set the address of option data to FFE0H.

DW 0002H ; Crystal oscillation circuit, 2 kHz sampling will not be carried out

- When the RC oscillation circuit is specified for the low-speed clock oscillation circuit and carrying out reset signal sampling is specified in the ML63193.

ORG FFE0H ; Use an assembler pseudo-instruction to set the address of option data to FFE0H.

DW 0001H ; RC oscillation circuit, 2 kHz sampling will be carried out

We, _____, hereby confirm that all the points stated above have been checked.

Signature

Date