



# **GMS90 Series**

# **Application Guide Sheet**



**HYUNDAI**  
MicroElectronics

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## 1. GMS90 Series Characteristics Improve Status

### GMS90 Series Characteristics Improve Status

Problem	Device							
	GMS90C52	GMS90C52B	GMS97C52	GMS97L52	GMS90C58	GMS97C58	GMS97C2051	GMS97L2051
AJMP ACALL	NO	YES	YES	YES	YES	YES	YES	YES
T2CON	NO	YES	NO	YES	YES	YES	-	-
<b>EMI</b>	NO	NO	NO	YES 450pF*	YES 1000pF*	YES 1000pF*	NO	YES
Status	Production	Production	Production	Production	Production	Production	Production	Production

Note : \* Built in capacitor to reduce EMI

Some customers complain that GMS90 Series are not completely compatible with MCS-51 Family products. As we already know, GMS90 Series are MCS-51 2<sup>nd</sup> source products designed based on Siemens Core. In function and operation, GMS90 Series are compatible with MCS-51 products, but in DC characteristics they aren't fully compliant with MCS-51 products and have own GMS90 Series characteristics.

Actually, various elements of DC characteristics such as I/O Port Size, Inverting Amplifier Size of Oscillator part, External Interrupt  $V_{TH}$  interval, and etc. are different from MCS-51 products, which means each semiconductor maker (HME, ATMEL, Philips, Winbond, and etc.) has different characteristics not only in GMS90 Series but also in MCS-51 2<sup>nd</sup> Source .

Generally, the difference of characteristics doesn't affect application system much, but very rarely can lead to unexpected result. For this reason, application engineer should be very careful in case that MCS-51 product is replaced with 2<sup>nd</sup> Source product or 2<sup>nd</sup> Source with 2<sup>nd</sup> Source mutually.

## 2. General Troubleshooting

When GMS90 Series doesn't perform start operation in application System, you should do troubleshooting by checking them in following order.

### 2.1. Power Check

Should check if the voltage supplied to Vcc part is stable or if it is in the range of MCU operating voltage.

### 2.2. XTAL1,XTAL2 Pin Check

Should check pin 18(Xtal2) and pin 19(Xtal1) if they oscillates synchronously with operating frequency. And check if Loading Capacitors C1, C2, and quartz crystal are set as close as possible to pin 18 and 19. In case of using quartz crystal, Loading Capacitors C1 and C2 use approximately 30pF value. In case of using ceramic resonator except quartz crystal, Loading Capacitors. C1 and C2 are recommended to use approximately 47pF value.

### 2.3. RESET Pin Check

Should check if Reset Time is enough. i.e. check if Reset is released after the oscillator is sufficiently stabilized. Should check the timing of oscillator part, Vcc part, and Reset part at the same time.

### 2.4. /EA (External Access enable) Pin Check

Should check if in Internal ROM Mode, /EA Pin is set to High(V<sub>CC</sub>), if in External ROM Mode(ROM-less), /EA Pin is set to Low(GND), and if in Internal + External ROM Mode, /EA Pin is set to High(V<sub>CC</sub>).

### 2.5. /PSEN Pin And ALE Pin Check

/PSEN pin and ALE pin should generate rectangular pulse regardless of ROM existence when they are used in External ROM Mode(ROM-less). When /PSEN and ALE are precisely synchronized and in case of using 12MHz quartz crystal, they have 2MHz frequency which is 1/6 frequency. Positive Duty Cycle of /PSEN is about 50% and Positive Duty Cycle of ALE is about 33.3%. If these signals aren't generated, /EA pin of CPU should be checked.

### 2.6. Direction Setting for I/O Port

All of 8 pins in each port can bidirectional I/O by the bit. To use it as an input, the bit should be read after written to '1'. In general application, once port direction is set to input/output, it is used without changing. But to use it as SDA line in I<sup>2</sup>C communication, input/output direction is changed continuously. When output is converted to input, if it is read without first written to "1", corresponding port can be damaged by over-electric current on chip or resultant chip heating.

### 2.7. Stack Pointer Setting

Should check in each device if Stack Pointer is assigned properly without overlapped RAM .

### 2.8. RAM Clear Check

Should check in program initialization process if RAM is cleared properly.

### 2.9. How much electric current per pin can be sunk?

In spec. it says that the external circuit should be designed with the maximum current per pin to sink to 10mA and limited within 100mA in total in the condition that pin is used continuously. If you want over 10mA LED direct drive, you should find proper current experimenting by yourself. Actually experimented result is appeared that it can be operated up to 15mA without any problem.

### 3. Beginner Troubleshooting

#### 3.1. Drive Capability Of The Internal Pullups

The pins of Ports 1,2, and 3 of the CMOS parts each have three pullups: strong, normal, and weak, as shown in Figure 3.1. The strong pullup (P1) is only used during 0-to-1 transitions, to hasten the transition. The weak pullup (P2) is on whenever the bit latch contains a 1. The “normal” pullup (P3) is controlled by the pin voltage itself.

The reason that P3 is controlled by the pin voltage is that if the pin is being used as an input, and the external source pulls it to a low, then turning off P3 makes for lower  $I_{IL}$ . The data sheet shows an “ $I_{IL}$ ” specification. This is the current that P3 will source during the time the pin voltage is making its 1-to-0 transition. This is what  $I_{IL}$  would be if an input low at the pin didn’t turn P3 off.

Note, however, that this P3 turn-off mechanism puts a restriction on the drive capacity of the pin if it’s being used as an output. If you’re trying to output a logic high, and the external load pulls the pin voltage below the pin’s  $V_{IH,MIN}$  spec, P3 might turn off, leaving only the weak P2 to provide drive to the load. To prevent this happening, you need to ensure that the load doesn’t draw more than the  $I_{OH}$  spec for a valid  $V_{OH}$ . The idea is to make sure the pin voltage never falls below its own  $V_{IH,MIN}$  specification.

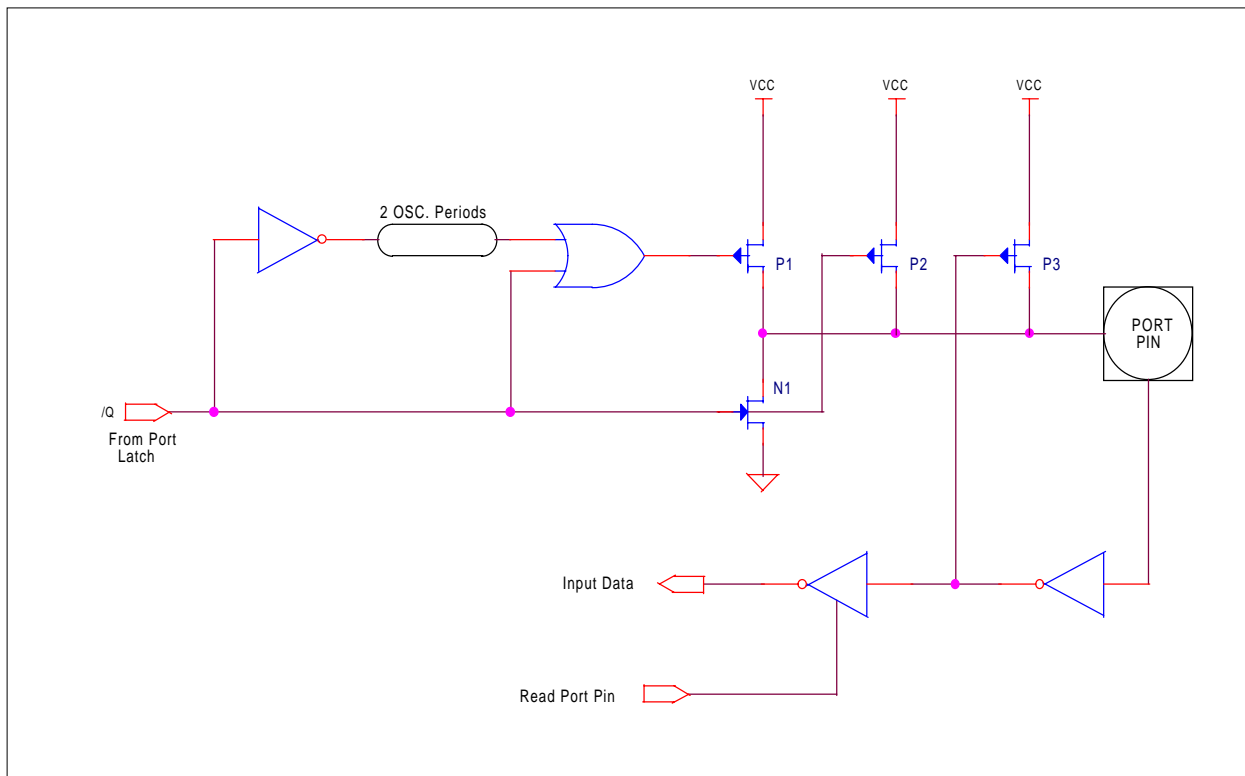


Figure 3.1 GMS90 Series Output Drivers For Ports 1,2 and 3

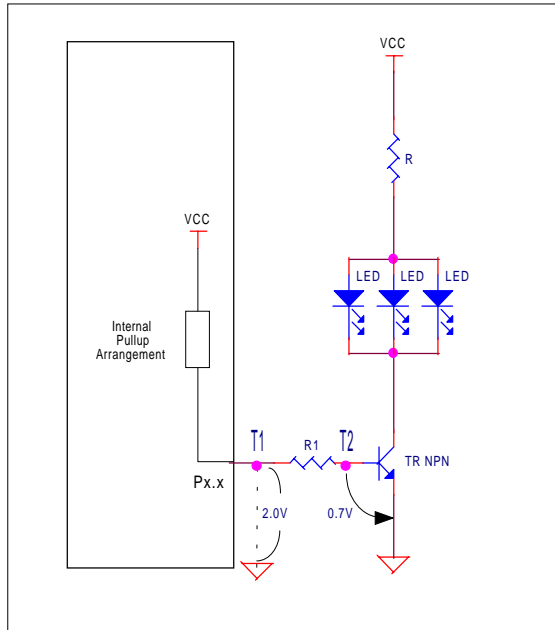


Figure 3.2 Problem occurring application

Then let's check what kind of problem can be occurred by this Output Driver Mechanism in customer application.

In general case, there is no specific problem. One of typical problem occurring type is shown in figure 3.2.

In this kind of application, when NPN Transistor is driven to High to turn on LED, the voltage of T1 point is located between 2V~5V. If the voltage of T1 point is fell down under 2.0V, P3 is turned off remaining only slight output current of P2, then NPN Transistor is turned Off to turn LED off consequently.

You should be very careful that the voltage of T1 point is appeared differently by the manufacturers because each manufacturer has different Internal Pull-up characteristics.

The solutions for this problem are as follows.

1. Add an external pull-up resistor as shown in figure 3.3.
2. Use Darlington Tr.
3. Use PNP Transistor of 'Active Low' as shown in figure 3.4.

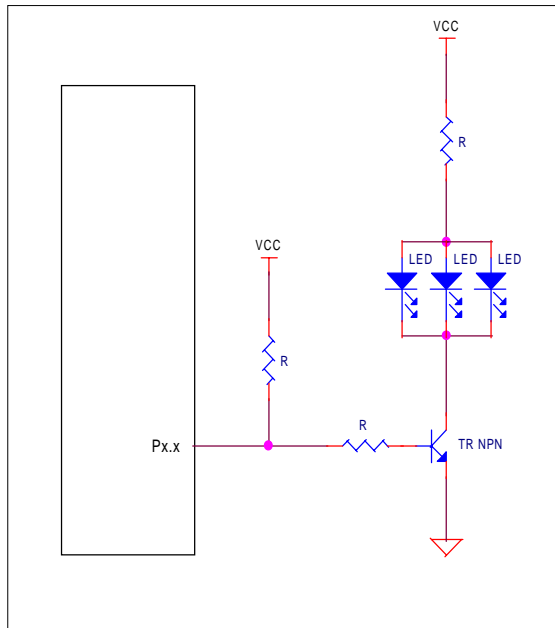


Figure 3.3 Use an additional external pullup resistor

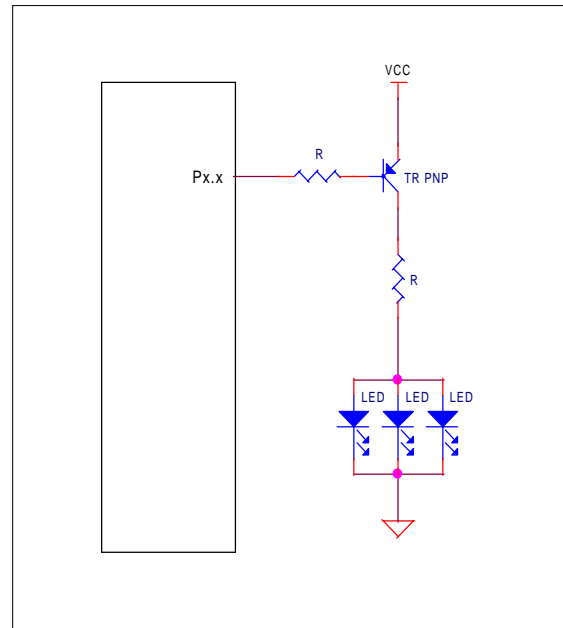


Figure 3.4 Use low output PNP Tr.

### 3.2. $V_{OH}$ vs. Internal Pullup Resistor Value

Port 1, 2, and 3 have internal Pull-ups, and Port0 has Open Drain output. Port0 doesn't use internal Pull-up when it is used as an general port, but when it accesses external memory and is asserted High, it uses internal Pull-up. The resistor used as internal Pull-up doesn't use general linear resistor but electronic field effect transistor. Therefore resistor value is changed by  $V_{OH}$  of each Port. Following table indicates the internal Pull-up values of Port 1, 2, and 3 by each semiconductor maker. The table value is only test value under our test condition.

$V_{OH}$  vs. Internal Pullup Resistor Value

$V_{OH}$	4.5V	4.0V	3.5V	3.0V	2.5V	2.0V
<b>GMS90C52</b>	8.9K	9.8K	10.7k	12k	14K	16.5K
<b>GMS90C52B</b>	6.9K	7.3K	8.1K	8.7K	9.7K	10.9K
<b>GMS97C52</b>	9.3K	9.8K	10.7K	12K	13K	-
<b>GMS90L52</b>	6.1K	6.5K	7.3K	8K	8.8K	10.2K
<b>GMS90C58</b>	7.4K	7.8K	8.6K	9.3K	10.1K	11.6K
<b>GMS97C58</b>	7.0K	7.5K	8.1K	8.7K	10.1K	11.7K
<b>Intel87C52</b>	5.8K	6.3K	6.9K	7.3K	8.6K	-
<b>Philips87C52</b>	7.3K	7.8K	8.6K	9.3K	10.1K	11.7K
<b>MHS80C51</b>	9.2K	10K	10.7K	12K	13K	14.6K
<b>Winbond78C32B</b>	5.2K	5.5K	6.0K	6.7K	7.3K	-

## 4. Advanced Troubleshooting

### 4.1. External Interrupts Input

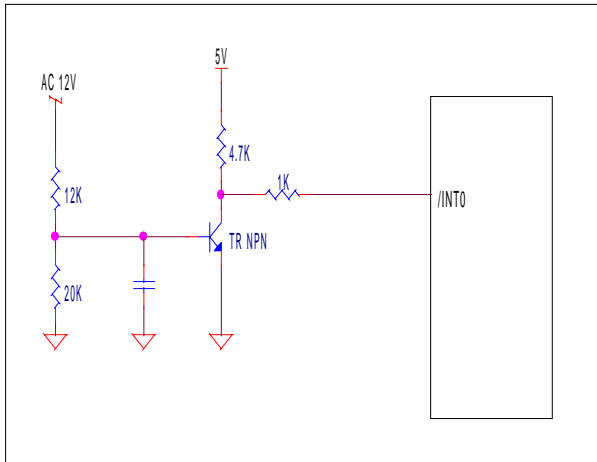


Figure 4.1 Circuit without C1

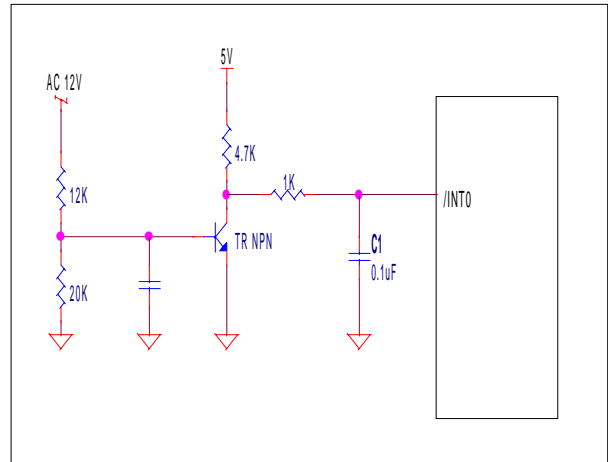


Figure 4.2 Circuit with C1

When you apply AC(60Hz/50Hz) power using as external Interrupt input source to time clock, Rising Time and Falling Time should be faster enough. The followings are the caution in circuit design.

In case of the circuit without C1 as shown in figure 4.1, it operates normally. But in case of using C1 as shown in figure 4.2, you will get unexpected result that time clock goes 2 or 3 times faster.

With C1 as shown in figure 4.2, 2~3 of Interrupts is generated in this section by making the Rising Time input to external Interrupt slow.

Figure 4.3 and 4.4 are the waveforms measured with program which toggles specific port in external Interrupt Service Routine when Interrupt is generated for Test at the Falling Edge.

Without C1 as shown in figure 4.3, normal result occurs that specific port toggles only at Falling Edge, but with C1 as shown in 4.4, abnormal result can occur that specific port toggles 2~3 times even at Rising Edge.

Figure 4.5 is the Rising Time without C1, and figure 4.6 is the Rising Time with C1.

As described in the following table, each semiconductor maker has difference of characteristics. But when Rising Time and/or Falling Time is longer than required time, 2~3 times faster time clock will be generated.

Device	Required Rising Time/Falling Time
GMS97C58	Faster than 20uS
Winbond W78C32B-40	Faster than 100uS
Intel P87C51	Faster than 250uS
MHS P80C32u-42	Faster than 300uS

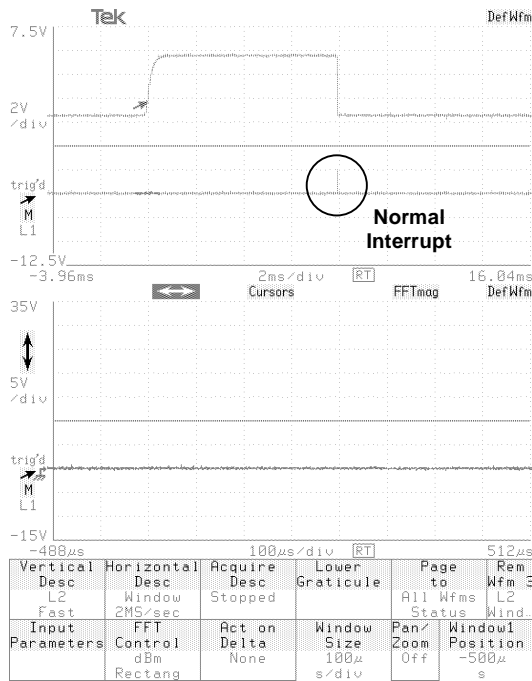


Figure4.3 Normal Interrupt

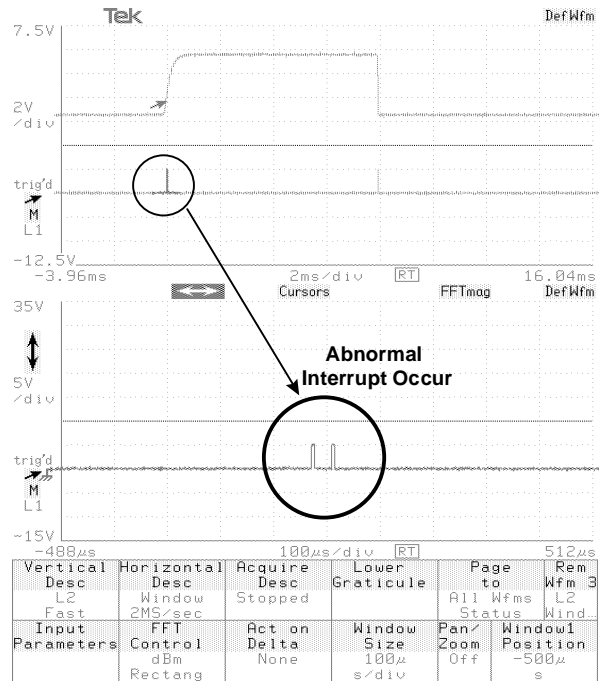


Figure 4.4 Abnormal Interrupt

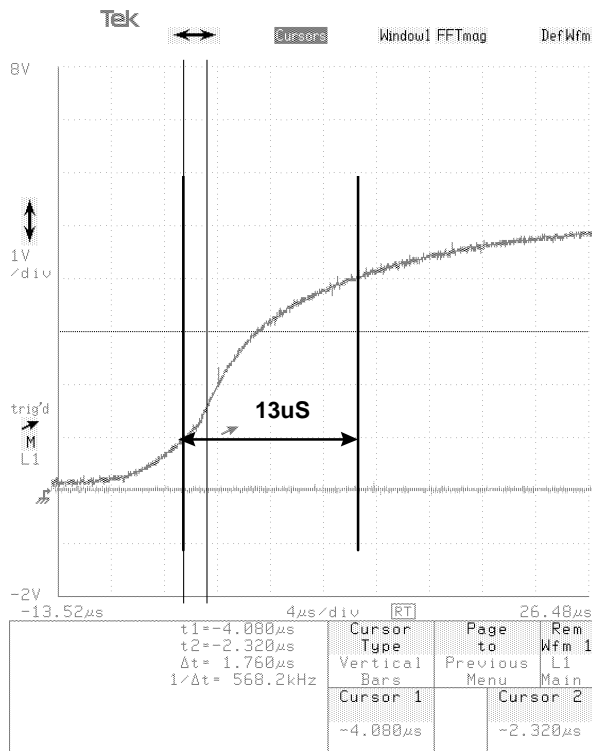


Figure4.5 When C1 Remove Rising Time

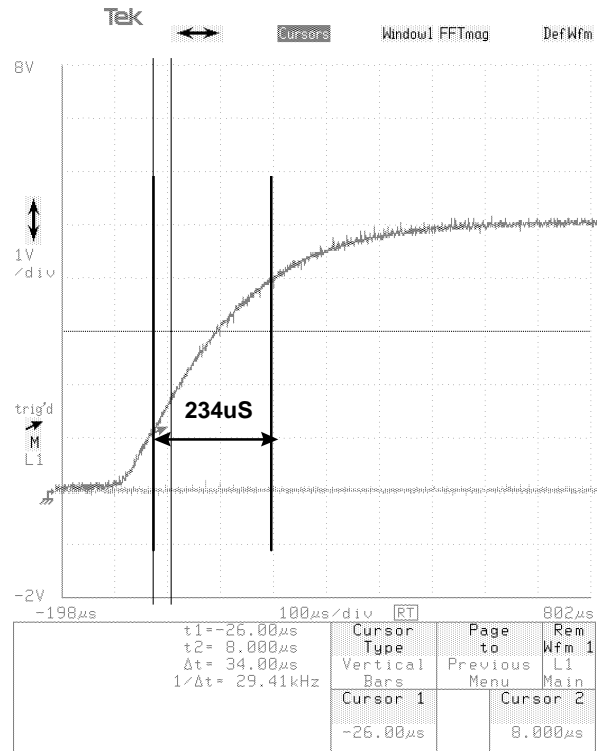


Figure 4.4 When C1 Use Rising Time



## 5. OTP Programming Troubleshooting

The reason of OTP programming fail should be checked in various ways. There can be various reasons such as some problems in programmer tool, contact disability by worn-out and/or oldness of Socket or TEXTTOOL, or mistakes of programmer due to the awkwardness of use, etc. If programming fail occurs while OTP programming, its mostly due to user's mistake. If programming fail occurs, first check following things.

1. Check if GMS90 Series programming algorithm is registered 3<sup>rd</sup> party programmer.
2. Check if Power is ON in programmer and interface with PC is set properly.
3. Check the connections of OTP, Adapter, and programmer in case of using socket adapter.
4. Try to program once more with the same code in case of OTP fail by connection errors.

## 6. GMS90 Series 3'rd Party Programmer

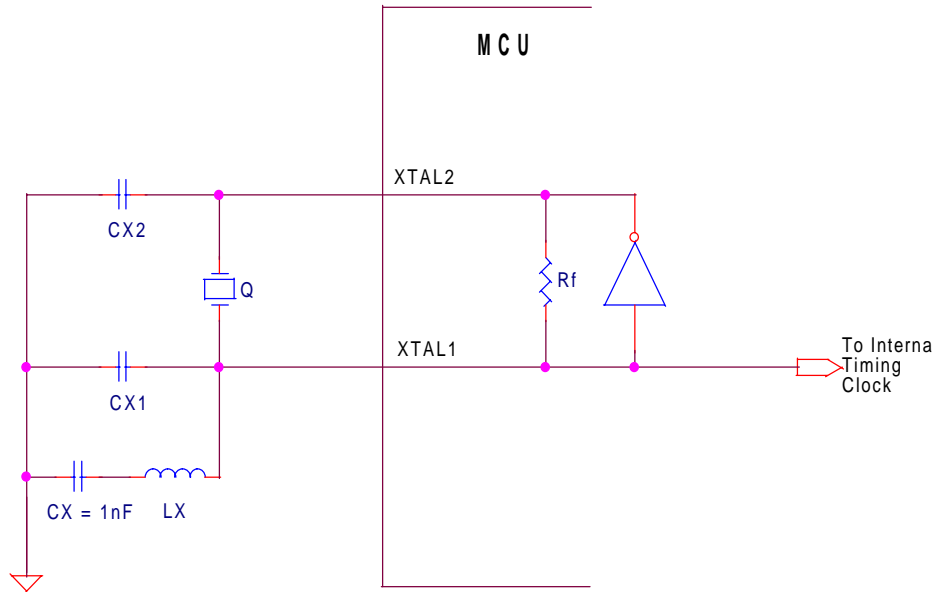
### GMS90 Series 3'rd Party Programmer List

COMPANY	ADVANTECH	Advin Systems, Inc	EETools	Ertec GmbH	HiLo Systems
<b>Http Address</b>	www.aec.com.tw	www.advin.com	www.eetools.com	www.ertec.com	www.hilosystems.com.tw
<b>PRODUCT</b>	LabTool-48 LabTool-408	PILOT-U128-Puls PILOT-U84-Puls PILOT-U448-Puls PILOT-MVP PILOT-145 PILOT-146	TopMax MegaMax AllMax+ ProMax RomMax	PGS53 PGS67	ALL-03A ALL-07 ALL-07A ALL-11 GANG-8
<b>Writing Available Device</b>	GMS97C/L51 GMS97C/L52 GMS97C/L54 GMS97C/L56 GMS97C/L58 GMS97C/L1051 GMS97C/L2051	GMS97C/L51 GMS97C/L52 GMS97C/L54 GMS97C/L56 GMS97C/L58 GMS97C/L58	GMS97C/L51 GMS97C/L52 GMS97C/L54 GMS97C/L56 GMS97C/L58 GMS97C/L1051 GMS97C/L2051	GMS97C/L51 GMS97C/L52 GMS97C/L54 GMS97C/L56 GMS97C/L58 GMS97C/L1051 GMS97C/L2051	GMS97C/L51 GMS97C/L52 GMS97C/L54 GMS97C/L56 GMS97C/L58 GMS97C/L1051 GMS97C/L2051

COMPANY	LEAP Electronic Co.	SMS GmbH	Stag Programmers	System General	XELTEK
<b>Http Address</b>	www.LEAP.com.tw	www.sms-sprint.com	www.stag.co.uk	www.sg.com.tw	www.xeltek.com
<b>PRODUCT</b>	LEAPER-10,6,5,3 SU-2000 LEAP-U1 LP-U4 LEAP-EP1 LEAP-Q5	Sprint Plus-48 Sprint Optima Sprint Multisyte	Eclipse Orbit32,48 P301,801,803 PH401 Solar Quasar1040,1084	Turpro-1,1/FX Turpro-1/TX Turpro-832,840 Turpro-848 Multi-Apro	Super-Pro
<b>Writing Available Device</b>	GMS97C/L51 GMS97C/L52 GMS97C/L54 GMS97C/L56 GMS97C/L58 GMS97C/L1051 GMS97C/L2051	GMS97C/L51 GMS97C/L52 GMS97C/L54 GMS97C/L56 GMS97C/L58 GMS97C/L1051 GMS97C/L2051	GMS97C/L51 GMS97C/L52 GMS97C/L54 GMS97C/L56 GMS97C/L58 GMS97C/L1051 GMS97C/L2051	GMS97C/L51 GMS97C/L52	GMS97C/L51 GMS97C/L52 GMS97C/L54 GMS97C/L56 GMS97C/L58 GMS97C/L1051 GMS97C/L2051

## 7. 3'rd Overtone Crystal Oscillator

### 7.1. Recommended Crystal Oscillator Circuits - 3'rd Overtone (@24 ~ 40MHz)



$$f_{LX,CX1} = \frac{1}{2\pi\sqrt{L_X \cdot C_{X1}}} \quad , \quad f_{LX,CX1} \approx \sqrt{f_{\text{FUNDAMENTAL}} \cdot f_{\text{3rd OVERTONE}}}$$

Example)

40MHz : CX1=15pF, CX2=10pF, LX=3uH

Q=13.333MHz 3'rd Overtone X-tal (Maybe Marked 40MHz)

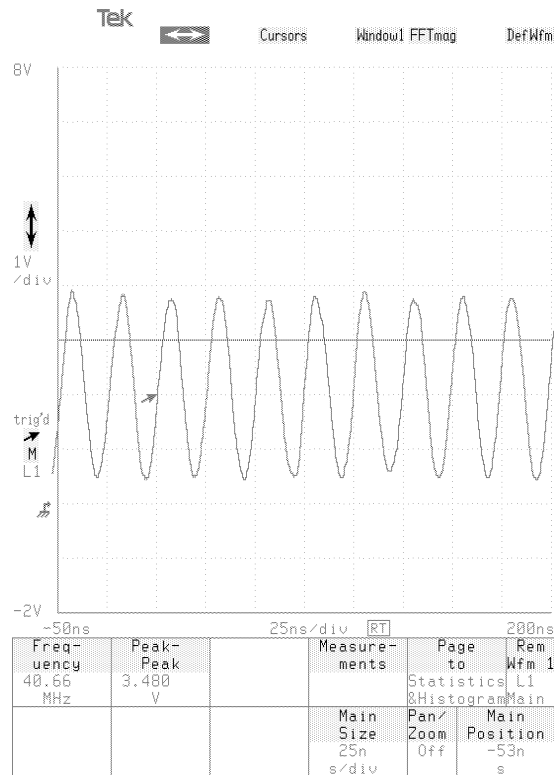
Startup time normally < 20mS for Vcc rise time < 2mS

Startup time significantly depending on quality of layout

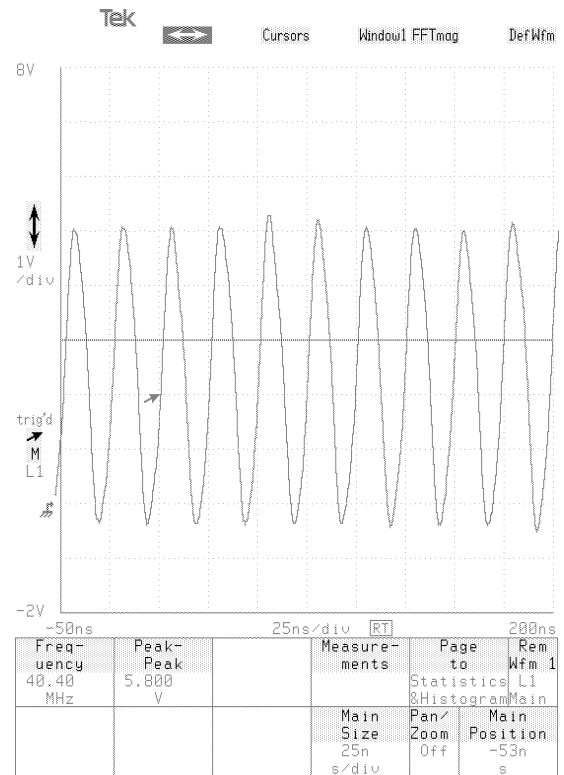
$$C_L = \frac{C_{X1\text{REST}} \cdot C_{X2}}{C_{X1\text{REST}} + C_{X2}} + C_{\text{STRAY}} \quad , \quad C_{X1\text{REST}} \approx C_{X1} - \frac{1}{(2\pi f)^2 \cdot L_X}$$

$C_{X2} = C_{X1\text{REST}}$  recommended ,

### 7.2. 40.5MHz 3'rd Overtone Oscillation Waveforms



XTAL1 Pin Waveform



XTAL2 Pin Waveform

Typical quartz crystal uses about 20MHz in fundamental frequency mode, in case that more frequency is oscillated, it is oscillated in harmonic mode called 3th, 5th, and 7th harmonic. Generally overtone oscillator is generated using LC resonance circuit(one-sided tank circuit), the case that overtone oscillator jumps to other mode to oscillate can happen if positive number setting is wrong(or not controlled precisely). Therefore if you want to oscillate overtone perfectly by using quartz crystal, you should use overtone use only IC, or in order to stable system clock you should use OSC(CAN Type) which embeds oscillator circuit.

## 8. GMS90 Series RC Reset Waveforms

@ R=10K, C=10uF

