

ML610Q411/Q412/Q415**Preliminary**

8-bit Microcontroller with a Built-in LCD driver

GENERAL DESCRIPTION

ML610Q411/Q412/Q415 is a high-performance 8-bit CMOS microcontroller into which rich peripheral circuits, such as synchronous serial port, UART, I²C bus interface (master), buzzer driver, battery level detect circuit, RC oscillation type A/D converter, 12-bit successive approximation type A/D converter, and LCD driver, are incorporated around OKI-original 8-bit CPU nX-U8/100.

The CPU nX-U8/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by 3-stage pipe line architecture parallel processing. The Flash ROM that is installed as program memory achieves low-voltage low-power consumption operation (read operation) equivalent to mask ROM and is most suitable for battery-driven applications. The on-chip debug function that is installed enables program debugging and programming.

ML610Q411/Q412 has a dual clock, runs at 32.768kHz crystal oscillation clock or a built-in 500kHz RC oscillation clock, used for a system requires the accurate clock or timer. ML610Q415 works with the built-in RC oscillation clock and does not need an external crystal oscillator, can lower a system cost and shrink the production board.

FEATURES

- CPU
 - 8-bit RISC CPU (CPU name: nX-U8/100)
 - Instruction system: 16-bit instructions
 - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
 - On-Chip debug function
 - Minimum instruction execution time
 - 30.5 μ s (@32.768 kHz system clock)
 - 2 μ s (@500kHz system clock)
- Internal memory
 - Internal 16KByte Flash ROM (8K \times 16 bits) (including unusable 1KByte TEST area)
 - Internal 1 KByte Data RAM (1024 \times 8 bits)
- Interrupt controller
 - 2 non-maskable interrupt sources
 - Internal source: 1 (Watch dog timer)
 - External source: 1 (NMI)
 - 19 maskable interrupt sources
 - Internal sources: 15 (SSIO, SA-A/D converter, I2C, Timer0, Timer1, Timer2, Timer3, 1kHz timer, UART, RC-A/D converter, PWM, TBC128Hz, TBC32Hz, TBC16Hz, TBC2Hz)
 - External sources: 4 (P00, P01, P02, P03)
- Time base counter
 - Low-speed time base counter \times 1 channel
 - Frequency compensation (Compensation range: Approx. -488 ppm to $+488$ ppm. Compensation accuracy: Approx. 0.48ppm)
 - High-speed time base counter \times 1 channel

- Watchdog timer
 - Non-maskable interrupt and reset
 - Free running
 - Overflow period: 4 types selectable
 - ML610Q411/Q412: 125ms, 500ms, 2s, and 8s
 - ML610Q415: approx. 131ms, 524ms, 2.1s, 8.4s
- Timers
 - 8 bits × 4 channels (Timer0-3: 16-bit x 2 configuration available by using Timer0-1 or Timer2-3)
 - Clock frequency measurement mode (in one channel of 16-bit configuration using Timer2-3, ML610Q415 does not have this mode)
- 1 kHz timer
 - Interrupt function
 - ML610Q411/Q412: 10 Hz/1 Hz interrupt
 - ML610Q415: 9.5Hz/0.95Hz interrupt
- Capture
 - Time base capture × 2 channels
 - ML610Q411/Q412: 4096 Hz to 32 Hz
 - ML610Q415: 3906Hz ~ 30.5H
- PWM
 - Resolution 16 bits × 1 channel
- Synchronous serial port
 - Master/slave selectable
 - LSB first/MSB first selectable
 - 8-bit length/16-bit length selectable
- UART
 - TXD/RXD × 1 channel
 - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
 - Positive logic/negative logic selectable
 - Built-in baud rate generator
- I²C bus interface
 - Master function only
 - Standard mode (50kbps)
- Buzzer driver
 - 4 output modes, 8 frequencies, 16 duty levels
- RC oscillation type A/D converter
 - 24-bit counter
 - Time division × 2 channels
- Successive approximation type A/D converter
 - 12-bit A/D converter
 - Input × 2 channels
 - Conversion time: 46us/1ch@500kHz
- General-purpose ports
 - Non-maskable interrupt input port × 1 channel
 - Input-only port × 6 channels (including secondary functions)
 - Output-only port × 3 channels (including secondary functions)
 - Input/output port
 - ML610Q411: 22 channels (including secondary functions)
 - ML610Q412: 14 channels (including secondary functions)
 - ML610Q415: 22 channels (including secondary functions)

- LCD driver
 - The number of segments
ML610Q411: 144 dots max. (36 seg × 4 com)
ML610Q412: 176 dots max. (44 seg × 4 com)
ML610Q415: 144 dots max. (36 seg × 4 com)
 - 1/1 to 1/4 duty
 - 1/3 bias (built-in bias generation circuit)
 - Frame frequency selectable
ML610Q411/Q412: approx. 64 Hz, 73 Hz, 85 Hz, and 102 Hz
ML610Q415: approx. 61 Hz, 70 Hz, 81 Hz, 97 Hz
 - Bias voltage multiplying clock selectable (8 types)
 - Contrast adjustment (32 steps)
 - LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable
- Reset
 - Reset through the RESET_N pin
 - Power-on reset generation when powered on
 - Reset when oscillation stop of the low-speed clock is detected (ML610Q415 does not have this function)
 - Reset by the watchdog timer (WDT) overflow
- Battery Level Detector
 - Threshold voltages: One of 16 levels
 - Accuracy: ±2% (Typ.)
- Clock
 - Low-speed clock
ML610Q411/ML610Q412: Crystal oscillation (32.768 kHz)
(This LSI can not guarantee the operation without low-speed crystal oscillation clock)
ML610Q415: 1/16 of Built-in RC oscillation 500 kHz (31.25 kHz)
(This LSI does not have low-speed crystal oscillation clock)
 - High-speed clock:
Built-in RC oscillation (500 kHz)
External clock (500 kHz or less)
 - High-speed Clock gear: 1/2 (250 kHz), 1/4 (125 kHz), 1/8 (62.5 kHz: default)
 - Selection of high-speed clock mode by software:
Built-in RC oscillation, External clock
- Power management
 - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
 - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
 - High-speed Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, 1/8 of the oscillation clock)
 - Block Control Function: Resets and completely turns circuits of unused peripherals off.
- Shipment
 - Chip
ML610Q411(P)-xxxWA (Blank product: ML610Q411(P)-NNNWA)
ML610Q412(P)-xxxWA (Blank product: ML610Q412(P)-NNNWA)
ML610Q415-xxxWA (Blank product: ML610Q415-NNNWA)
 - 120-pin plastic LQFP
ML610Q411(P)-xxxTBZ03A (Blank product: ML610Q411(P)-NNNTBZ03A)
ML610Q412(P)-xxxTBZ03A (Blank product: ML610Q412(P)-NNNTBZ03A)
ML610Q415-xxxTBZ03A (Blank product: ML610Q415-NNNTBZ03A)
xxx: ROM code number
P: Wide range temperature version
- Guaranteed operating range
 - Operating temperature: -20°C to +70°C (P version: -40°C to +85°C)
 - Operating voltage: $V_{DD} = 1.1V$ to 3.6V, $AV_{DD} = 2.2V$ to 3.6V

BLOCK DIAGRAM
ML610Q411/ML610Q415 Block Diagram

Figure 1 show the block diagram of the ML610Q411.
 "*" indicates the secondary function of each port.
 "**" indicates ML610Q415 does not have the crystal oscillation.

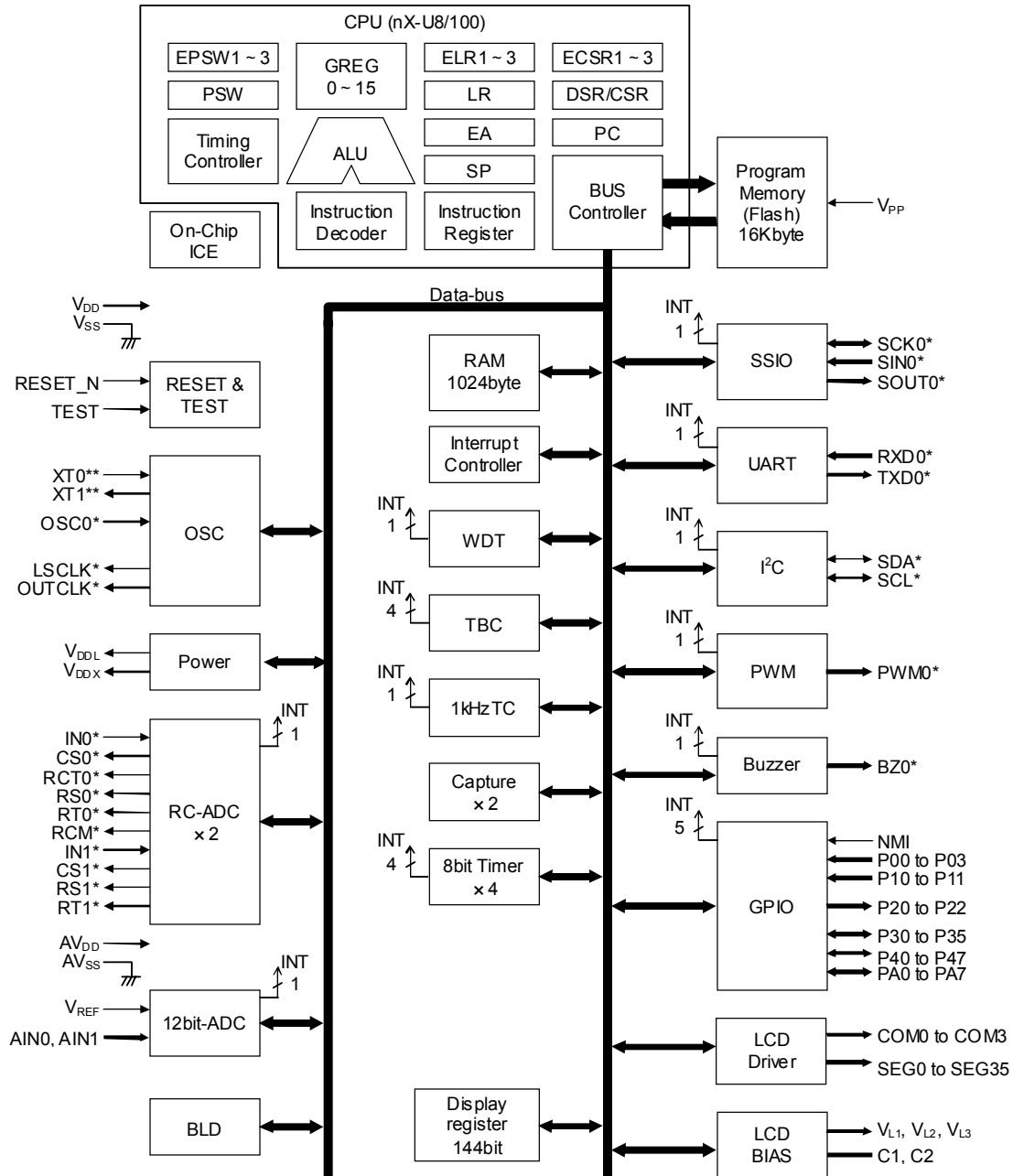


Figure 1 ML610Q411/ML610Q415 Block Diagram

ML610Q412 Block Diagram

Figure 2 show the block diagram of the ML610Q412.
 "*" indicates the secondary function of each port.

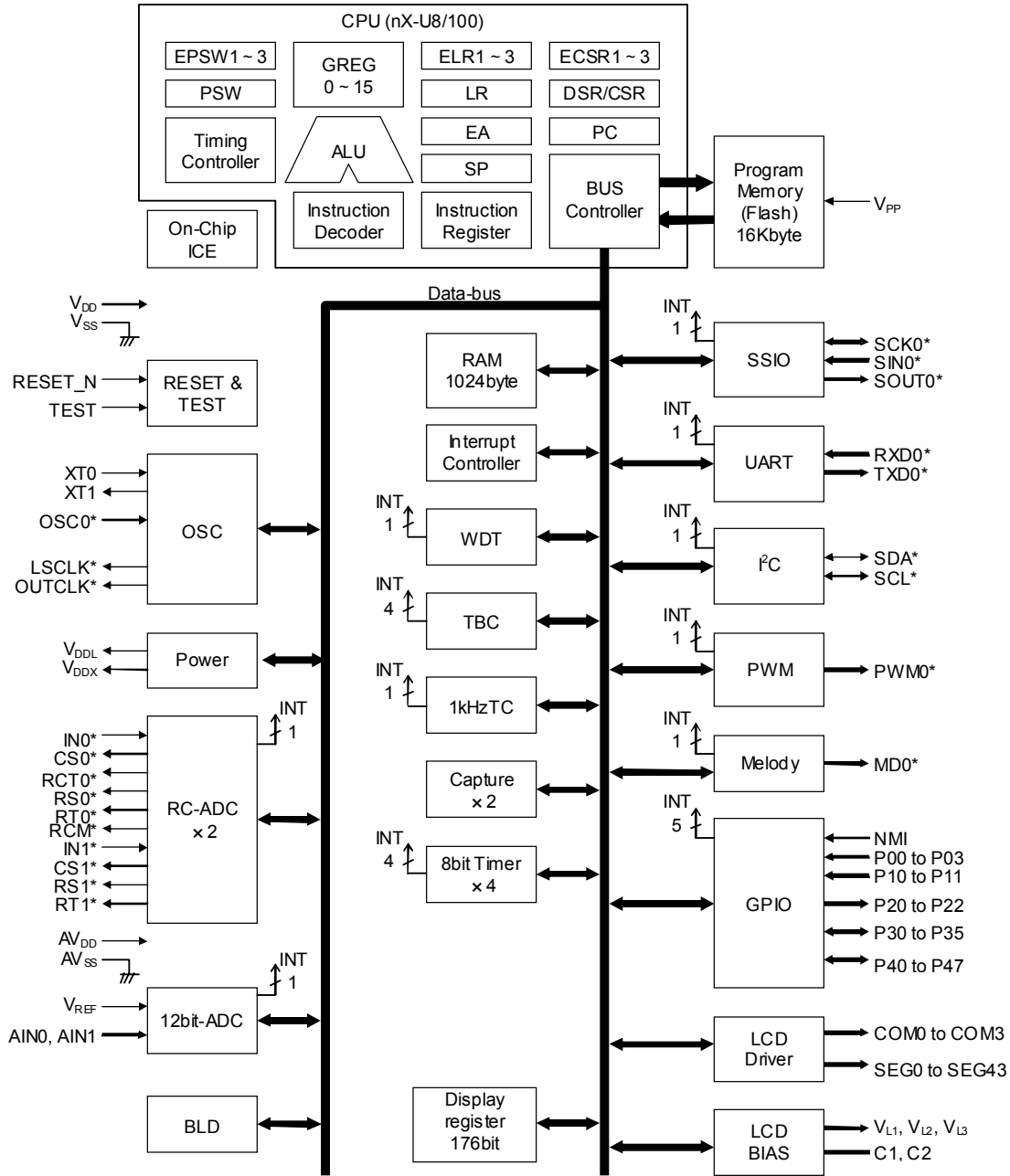


Figure 2 ML610Q412 Block Diagram

ML610Q412 TQFP120 Pin Layout

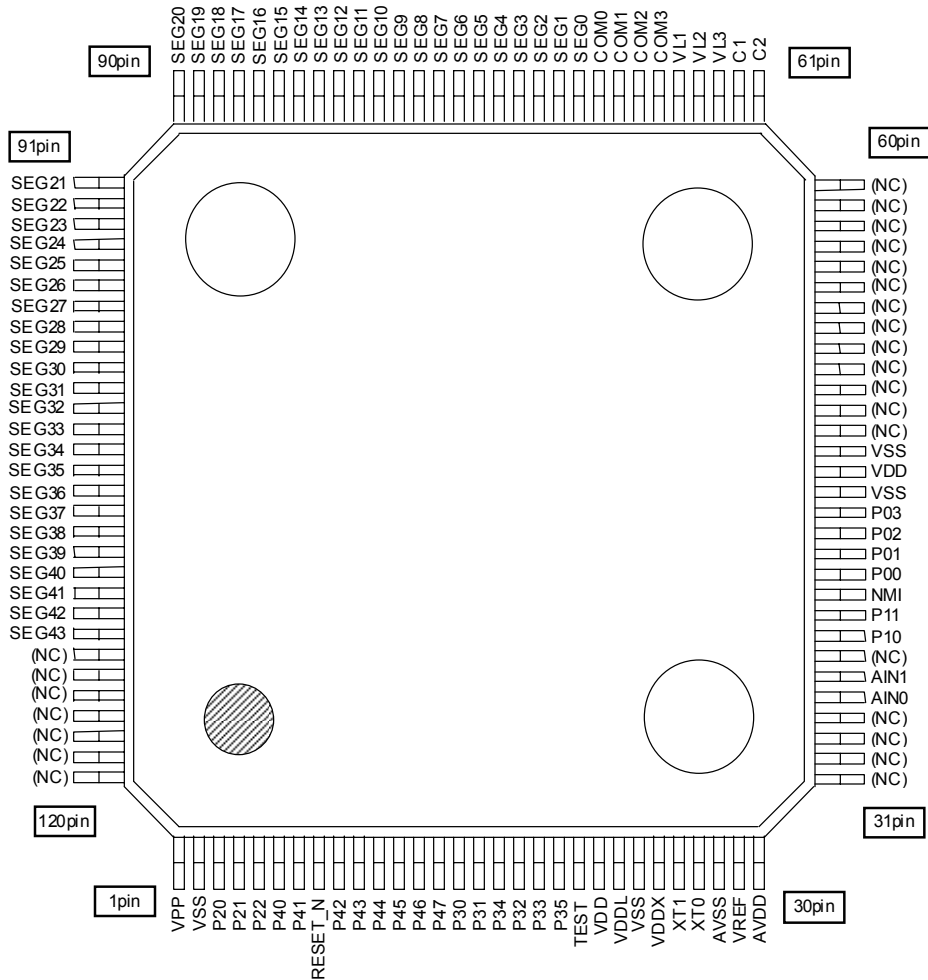
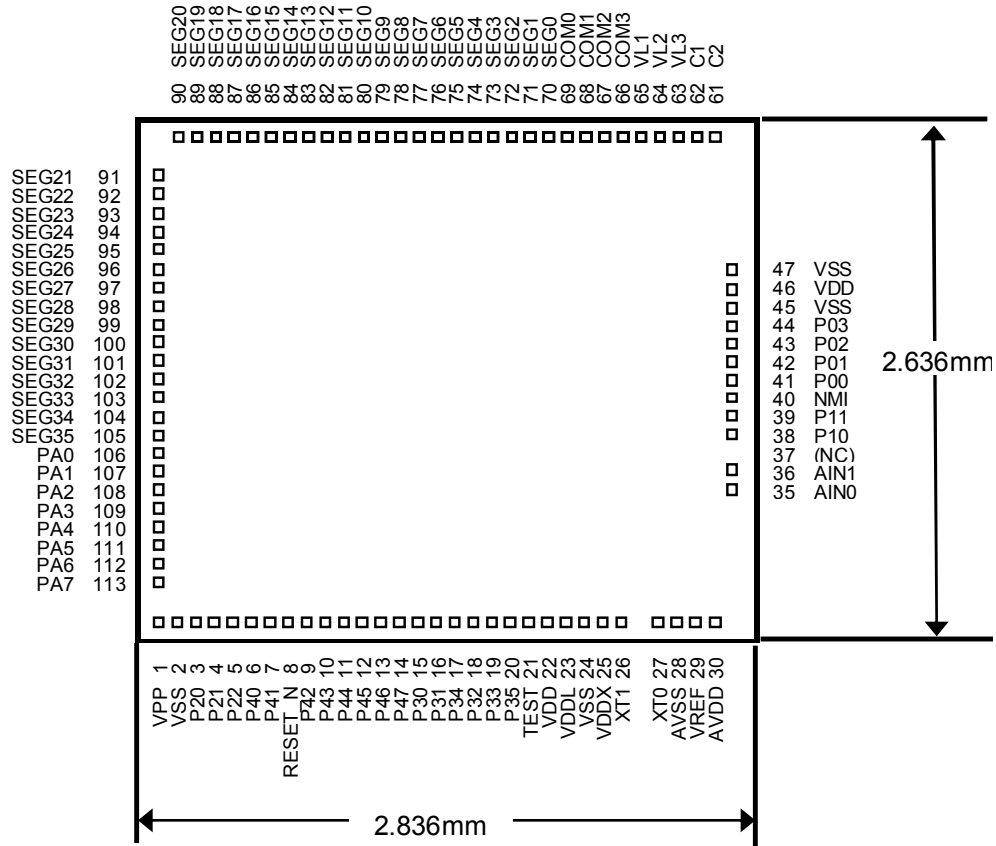


Figure 4 ML610Q412 TQFP120 Pin Configuration

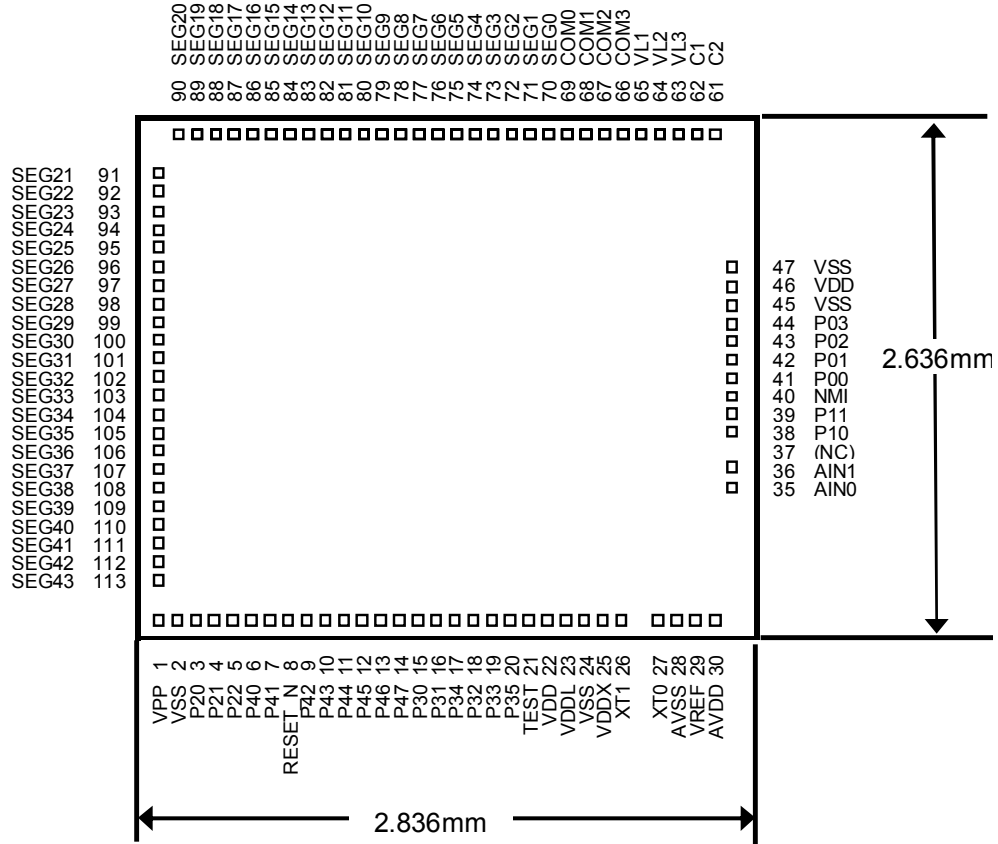
ML610Q411/ML610Q415 Chip Pin Layout & Dimension



Chip size: 2.836mm x 2.636mm
 PAD count: 95 pins
 Minimum PAD pitch: 80 μm
 PAD aperture: 70 μm × 70 μm
 Chip thickness: 350 μm
 Voltage of the rear side of chip: V_{SS} level

Figure 5 ML610Q411/ML610Q415 Chip Layout & Dimension

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Figure 6 ML610Q412 Chip Layout & Dimension

ML610Q411/ML610Q415 Pad Coordinates

Table 1 ML610Q411 Pad Coordinates

Chip Center: X=0,Y=0

PAD No.	Pad Name	X (μm)	Y (μm)	PAD No.	Pad Name	X (μm)	Y (μm)	PAD No.	Pad Name	X (μm)	Y (μm)
1	VPP	-1230	-1212	51	(NC)	-	-	101	SEG31	-1312	160
2	VSS	-1150	-1212	52	(NC)	-	-	102	SEG32	-1312	80
3	P20	-1070	-1212	53	(NC)	-	-	103	SEG33	-1312	0
4	P21	-990	-1212	54	(NC)	-	-	104	SEG34	-1312	-80
5	P22	-910	-1212	55	(NC)	-	-	105	SEG35	-1312	-160
6	P40	-830	-1212	56	(NC)	-	-	106	PA0	-1312	-240
7	P41	-750	-1212	57	(NC)	-	-	107	PA1	-1312	-320
8	RESET_N	-670	-1212	58	(NC)	-	-	108	PA2	-1312	-400
9	P42	-590	-1212	59	(NC)	-	-	109	PA3	-1312	-480
10	P43	-510	-1212	60	(NC)	-	-	110	PA4	-1312	-560
11	P44	-430	-1212	61	C2	1220	1212	111	PA5	-1312	-640
12	P45	-350	-1212	62	C1	1140	1212	112	PA6	-1312	-720
13	P46	-270	-1212	63	VL3	1060	1212	113	PA7	-1312	-800
14	P47	-190	-1212	64	VL2	980	1212	114	(NC)	-	-
15	P30	-110	-1212	65	VL1	900	1212	115	(NC)	-	-
16	P31	-30	-1212	66	COM3	820	1212	116	(NC)	-	-
17	P34	50	-1212	67	COM2	740	1212	117	(NC)	-	-
18	P32	130	-1212	68	COM1	660	1212	118	(NC)	-	-
19	P33	210	-1212	69	COM0	580	1212	119	(NC)	-	-
20	P35	290	-1212	70	SEGO	500	1212	120	(NC)	-	-
21	TEST	370	-1212	71	SEG1	420	1212				
22	VDD	450	-1212	72	SEG2	340	1212				
23	VDDL	530	-1212	73	SEG3	260	1212				
24	VSS	610	-1212	74	SEG4	180	1212				
25	VDDX	690	-1212	75	SEG5	100	1212				
26	XT1	770	-1212	76	SEG6	20	1212				
27	XTO	930	-1212	77	SEG7	-60	1212				
28	AVSS	1030	-1212	78	SEG8	-140	1212				
29	VREF	1110	-1212	79	SEG9	-220	1212				
30	AVDD	1190	-1212	80	SEG10	-300	1212				
31	(NC)	-	-	81	SEG11	-380	1212				
32	(NC)	-	-	82	SEG12	-460	1212				
33	(NC)	-	-	83	SEG13	-540	1212				
34	(NC)	-	-	84	SEG14	-620	1212				
35	AIN0	1312	-522	85	SEG15	-700	1212				
36	AIN1	1312	-350	86	SEG16	-780	1212				
37	(NC)	-	-	87	SEG17	-860	1212				
38	P10	1312	-210	88	SEG18	-940	1212				
39	P11	1312	-130	89	SEG19	-1020	1212				
40	NMI	1312	-50	90	SEG20	-1100	1212				
41	P00	1312	30	91	SEG21	-1312	960				
42	P01	1312	110	92	SEG22	-1312	880				
43	P02	1312	190	93	SEG23	-1312	800				
44	P03	1312	270	94	SEG24	-1312	720				
45	VSS	1312	350	95	SEG25	-1312	640				
46	VDD	1312	430	96	SEG26	-1312	560				
47	VSS	1312	510	97	SEG27	-1312	480				
48	(NC)	-	-	98	SEG28	-1312	400				
49	(NC)	-	-	99	SEG29	-1312	320				
50	(NC)	-	-	100	SEG30	-1312	240				

ML610Q412 Pad Coordinates

Table 2 ML610Q412 Pad Coordinates

Chip Center: X=0,Y=0

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4	P21	-990	-1212	54	(NC)	-	-	104	SEG34	-1312	-80
5	P22	-910	-1212	55	(NC)	-	-	105	SEG35	-1312	-160
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8	RESET_N	-670	-1212	58	(NC)	-	-	108	SEG38	-1312	-400
9	P42	-590	-1212	59	(NC)	-	-	109	SEG39	-1312	-480
10	P43	-510	-1212	60	(NC)	-	-	110	SEG40	-1312	-560
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14	P47	-190	-1212	64	VL2	980	1212	114	(NC)	-	-
15	P30	-110	-1212	65	VL1	900	1212	115	(NC)	-	-
16	P31	-30	-1212	66	COM3	820	1212	116	(NC)	-	-
17	P34	50	-1212	67	COM2	740	1212	117	(NC)	-	-
18	P32	130	-1212	68	COM1	660	1212	118	(NC)	-	-
19	P33	210	-1212	69	COM0	580	1212	119	(NC)	-	-
20	P35	290	-1212	70	SEG0	500	1212	120	(NC)	-	-
21	TEST	370	-1212	71	SEG1	420	1212				
22	VDD	450	-1212	72	SEG2	340	1212				
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27	XTO	930	-1212	77	SEG7	-60	1212				
28	AVSS	1030	-1212	78	SEG8	-140	1212				
29	VREF	1110	-1212	79	SEG9	-220	1212				
30	AVDD	1190	-1212	80	SEG10	-300	1212				
31	(NC)	-	-	81	SEG11	-380	1212				
32	(NC)	-	-	82	SEG12	-460	1212				
33	(NC)	-	-	83	SEG13	-540	1212				
34	(NC)	-	-	84	SEG14	-620	1212				
35	AIN0	1312	-522	85	SEG15	-700	1212				
36	AIN1	1312	-350	86	SEG16	-780	1212				
37	(NC)	-	-	87	SEG17	-860	1212				
38	P10	1312	-210	88	SEG18	-940	1212				
39	P11	1312	-130	89	SEG19	-1020	1212				
40	NMI	1312	-50	90	SEG20	-1100	1212				
41	P00	1312	30	91	SEG21	-1312	960				
42	P01	1312	110	92	SEG22	-1312	880				
43	P02	1312	190	93	SEG23	-1312	800				
44	P03	1312	270	94	SEG24	-1312	720				
45	VSS	1312	350	95	SEG25	-1312	640				
46	VDD	1312	430	96	SEG26	-1312	560				
47	VSS	1312	510	97	SEG27	-1312	480				
48	(NC)	-	-	98	SEG28	-1312	400				
49	(NC)	-	-	99	SEG29	-1312	320				
50	(NC)	-	-	100	SEG30	-1312	240				

PIN LIST

PAD No.	Primary function			Secondary function			Tertiary function		
	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
2, 24,45,47	V _{SS}	—	Negative power supply pin	—	—	—	—	—	—
22, 46	V _{DD}	—	Positive power supply pin	—	—	—	—	—	—
23	V _{DDL}	—	Power supply pin for internal logic (internally generated)	—	—	—	—	—	—
25	V _{DDX}	—	Power supply pin for low-speed oscillation (internally generated)	—	—	—	—	—	—
1	V _{PP}	—	Power supply pin for Flash ROM	—	—	—	—	—	—
28	AV _{SS}	—	Negative power supply pin for successive approximation type ADC	—	—	—	—	—	—
30	AV _{DD}	—	Positive power supply pin for successive approximation type ADC	—	—	—	—	—	—
65	V _{L1}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
64	V _{L2}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
63	V _{L3}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
62	C1	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
61	C2	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
21	TEST	I/O	Input/output pin for testing	—	—	—	—	—	—
8	RESET_N	I	Reset input pin	—	—	—	—	—	—
27	XT0(*3)	I	Low-speed clock oscillation pin	—	—	—	—	—	—
26	XT1(*3)	O	Low-speed clock oscillation pin	—	—	—	—	—	—
29	V _{REF}	—	Reference power supply pin for successive approximation type ADC	—	—	—	—	—	—

PAD No.	Primary function			Secondary function			Tertiary function		
	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
36	AIN0	I	Successive approximation type ADC input	—	—	—	—	—	—
37	AIN1	I	Successive approximation type ADC input	—	—	—	—	—	—
40	NMI	I	Non-maskable interrupt pin	—	—	—	—	—	—
41	P00/EXI0/ CAP0	I	Input port, External interrupt 0, Capture 0 input	—	—	—	—	—	—
42	P01/EXI1/ CAP1	I	Input port, External interrupt 1, Capture 1 input	—	—	—	—	—	—
43	P02/EXI2/ RXD0	I	Input port, External interrupt 2, UART0 receive	—	—	—	—	—	—
44	P03/EXI3	I	Input port, External interrupt 3	—	—	—	—	—	—
38	P10	I	Input port	OSC0	I	High-speed oscillation	—	—	—
39	P11	I	Input port	—	—	—	—	—	—
3	P20/LED0	O	Output port	LSCLK	O	Low-speed clock output	—	—	—
4	P21/LED1	O	Output port	OUTCLK	O	High-speed clock output	—	—	—
5	P22/LED2	O	Output port	MD0	O	Melody output	—	—	—
15	P30	I/O	Input/output port	IN0	I	RC type ADC0 oscillation input pin	—	—	—
16	P31	I/O	Input/output port	CS0	O	RC type ADC0 reference capacitor connection pin	—	—	—
17	P34	I/O	Input/output port	RCT0	O	RC type ADC0 resistor/capacitor sensor connection pin	PWM0	O	PWM output
18	P32	I/O	Input/output port	RS0	O	RC type ADC0 reference resistor connection pin	—	—	—
19	P33	I/O	Input/output port	RT0	O	RC type ADC0 resistor sensor connection pin	—	—	—
20	P35	I/O	Input/output port	RCM	O	RC type ADC oscillation monitor	—	—	—
6	P40	I/O	Input/output port	SDA	I/O	I ² C data input/output	SIN0	I	SSIO data input
7	P41	I/O	Input/output port	SCL	I/O	I ² C clock input/output	SCK0	I/O	SSIO synchronous clock
9	P42	I/O	Input/output port	RXD0	I	UART data input	SOUT0	I	SSIO data output
10	P43	I/O	Input/output port	TXD0	O	UART data output	PWM0	O	PWM output
11	P44/T02P0 CK	I/O	Input/output port, Timer 0/Timer 2/PWM0 external clock input	IN1	I	RC type ADC1 oscillation input pin	SIN0	I	SSIO0 data input
12	P45/T13P1 CK	I/O	Input/output port, Timer 1/Timer 3 external clock input	CS1	O	RC type ADC1 reference capacitor connection pin	SCK0	I/O	SSIO0 synchronous clock
13	P46	I/O	Input/output port	RS1	O	RC type ADC1 reference resistor connection pin	SOUT0	O	SSIO0 data output
14	P47	I/O	Input/output port	RT1	O	RC type ADC1 resistor sensor connection pin	—	—	—
106	PA0 ^(*1)	I/O	Input/output port	—	—	—	—	—	—
	SEG36 ^(*2)	O	LCD segment pin	—	—	—	—	—	—
107	PA1 ^(*1)	I/O	Input/output port	—	—	—	—	—	—
	SEG37 ^(*2)	O	LCD segment pin	—	—	—	—	—	—
108	PA2 ^(*1)	I/O	Input/output port	—	—	—	—	—	—
	SEG38 ^(*2)	O	LCD segment pin	—	—	—	—	—	—
109	PA3 ^(*1)	I/O	Input/output port	—	—	—	—	—	—
	SEG39 ^(*2)	O	LCD segment pin	—	—	—	—	—	—

PAD No.	Primary function			Secondary function			Tertiary function		
	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
110	PA4 ^{(*)1}	I/O	Input/output port	—	—	—	—	—	—
	SEG40 ^{(*)2}	O	LCD segment pin	—	—	—	—	—	—
111	PA5 ^{(*)1}	I/O	Input/output port	—	—	—	—	—	—
	SEG41 ^{(*)2}	O	LCD segment pin	—	—	—	—	—	—
112	PA6 ^{(*)1}	I/O	Input/output port	—	—	—	—	—	—
	SEG42 ^{(*)2}	O	LCD segment pin	—	—	—	—	—	—
113	PA7 ^{(*)1}	I/O	Input/output port	—	—	—	—	—	—
	SEG43 ^{(*)2}	O	LCD segment pin	—	—	—	—	—	—
69	COM0	O	LCD common pin	—	—	—	—	—	—
68	COM1	O	LCD common pin	—	—	—	—	—	—
67	COM2	O	LCD common pin	—	—	—	—	—	—
66	COM3	O	LCD common pin	—	—	—	—	—	—
70	SEG0	O	LCD segment pin	—	—	—	—	—	—
71	SEG1	O	LCD segment pin	—	—	—	—	—	—
72	SEG2	O	LCD segment pin	—	—	—	—	—	—
73	SEG3	O	LCD segment pin	—	—	—	—	—	—
74	SEG4	O	LCD segment pin	—	—	—	—	—	—
75	SEG5	O	LCD segment pin	—	—	—	—	—	—
76	SEG6	O	LCD segment pin	—	—	—	—	—	—
77	SEG7	O	LCD segment pin	—	—	—	—	—	—
78	SEG8	O	LCD segment pin	—	—	—	—	—	—
79	SEG9	O	LCD segment pin	—	—	—	—	—	—
80	SEG10	O	LCD segment pin	—	—	—	—	—	—
81	SEG11	O	LCD segment pin	—	—	—	—	—	—
82	SEG12	O	LCD segment pin	—	—	—	—	—	—
83	SEG13	O	LCD segment pin	—	—	—	—	—	—
84	SEG14	O	LCD segment pin	—	—	—	—	—	—
85	SEG15	O	LCD segment pin	—	—	—	—	—	—
86	SEG16	O	LCD segment pin	—	—	—	—	—	—
87	SEG17	O	LCD segment pin	—	—	—	—	—	—
88	SEG18	O	LCD segment pin	—	—	—	—	—	—
89	SEG19	O	LCD segment pin	—	—	—	—	—	—
90	SEG20	O	LCD segment pin	—	—	—	—	—	—
91	SEG21	O	LCD segment pin	—	—	—	—	—	—
92	SEG22	O	LCD segment pin	—	—	—	—	—	—
93	SEG23	O	LCD segment pin	—	—	—	—	—	—
94	SEG24	O	LCD segment pin	—	—	—	—	—	—
95	SEG25	O	LCD segment pin	—	—	—	—	—	—
96	SEG26	O	LCD segment pin	—	—	—	—	—	—
97	SEG27	O	LCD segment pin	—	—	—	—	—	—
98	SEG28	O	LCD segment pin	—	—	—	—	—	—
99	SEG29	O	LCD segment pin	—	—	—	—	—	—
100	SEG30	O	LCD segment pin	—	—	—	—	—	—
101	SEG31	O	LCD segment pin	—	—	—	—	—	—
102	SEG32	O	LCD segment pin	—	—	—	—	—	—
103	SEG33	O	LCD segment pin	—	—	—	—	—	—
104	SEG34	O	LCD segment pin	—	—	—	—	—	—
105	SEG35	O	LCD segment pin	—	—	—	—	—	—

(*)1) Pins on ML610Q411 and ML610Q415.

(*)2) Pins on ML610Q412.

(*)3) ML610Q415 does not have the low-speed crystal oscillation function, but XT0 pin must be tied to V_{SS}.

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a "L" level, system reset mode is set and the internal section is initialized. When this pin is set to a "H" level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
XT0	I	Crystal connection pin for low-speed clock.	—	—
XT1	O	A 32.768 kHz crystal oscillator (see measuring circuit 1) is connected to this pin. Capacitors CDL and CGL are connected across this pin and V _{SS} as required. ML610Q415 does not have the crystal oscillation function, but connect XT0 to VSS and non-connect XT1 on ML610Q415.	—	—
OSC0	I	High-speed external clock input pin. This pin is used as the secondary function of the P10.	Secondary	—
LSCLK	O	Low-speed clock output pin. This pin is used as the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the secondary function of the P21 pin.	Secondary	—
General-purpose input port				
P00-P03	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P10-P11	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose output port				
P20-P22	O	General-purpose output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose input/output port				
P30-P35	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P40-P47	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
PA0-PA7	I/O	General-purpose input/output port. These pins are for the ML610Q411 and ML610Q415, but are not provided in the ML610Q412.	Primary	Positive

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
UART				
TXD0	O	UART data output pin. This pin is used as the secondary function of the P43 pin.	Secondary	Positive
RXD0	I	UART data input pin. This pin is used as the secondary function of the P42 or the primary function of the P02 pin.	Primary/Secondary	Positive
I²C bus interface				
SDA	I/O	I ² C data input/output pin. This pin is used as the secondary function of the P40 pin. This pin has an NMOS open drain output. When using this pin as a function of the I ² C, externally connect a pull-up resistor.	Secondary	Positive
SCL	O	I ² C clock output pin. This pin is used as the secondary function of the P41 pin. This pin has an NMOS open drain output. When using this pin as a function of the I ² C, externally connect a pull-up resistor.	Secondary	Positive
Synchronous serial (SSIO)				
SCK0	I/O	Synchronous serial clock input/output pin. This pin is used as the tertiary function of the P41 or P45 pin.	Tertiary	—
SIN0	I	Synchronous serial data input pin. This pin is used as the tertiary function of the P40 or P44 pin.	Tertiary	Positive
SOUT0	O	Synchronous serial data output pin. This pin is used as the tertiary function of the P42 or P46 pin.	Tertiary	Positive
PWM				
PWM0	O	PWM0 output pin. This pin is used as the tertiary function of the P43 or P34 pin.	Tertiary	Positive
T02P0CK	O	PWM0 external clock input pin. This pin is used as the primary function of the P44 pin.	Primary	—
External interrupt				
NMI	I	External non-maskable interrupt input pin. An interrupt is generated on both edges.	Primary	Positive/negative
EXI0-3	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P00-P03 pins.	Primary	Positive/negative
Capture				
CAP0	I	Capture trigger input pins. The value of the time base counter is captured in the register synchronously with the interrupt edge selected by software. These pins are used as the primary functions of the P00 pin(CAP0) and P01 pin(CAP1).	Primary	Positive/negative
CAP1	I		Primary	Positive/negative
Timer				
T02P0CK	I	External clock input pin used for both Timer 0 and Timer 2. The clocks for these timers are selected by software. This pin is used as the primary function of the P44 pin.	Primary	—
T13P1CK	I	External clock input pin used for both Timer 1 and Timer 3. The clocks for these timers are selected by software. This pin is used as the primary function of the P45 pin.	Primary	—
Buzzer				
BZ0	O	Buzzer signal output pin. This pin is used as the secondary function of the P22 pin.	Secondary	Positive/negative
LED drive				
LED0-2	O	NMOS open drain output pins to drive LED. These pins are used as the primary function of the P20-P22 pins.	Primary	Positive/negative

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
RC oscillation type A/D converter				
IN0	I	Channel 0 oscillation input pin. This pin is used as the secondary function of the P30 pin.	Secondary	—
CS0	O	Channel 0 reference capacitor connection pin. This pin is used as the secondary function of the P31 pin.	Secondary	—
RC T0	O	Resistor/capacitor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P33 pin.	Secondary	—
RS0	O	This pin is used as the secondary function of the P32 pin which is the reference resistor connection pin of Channel 0.	Secondary	—
RT0	O	Resistor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P34 pin.	Secondary	—
RCM	O	RC oscillation monitor pin. This pin is used as the secondary function of the P35 pin.	Secondary	—
IN1	I	Oscillation input pin of Channel 1. This pin is used as the secondary function of the P44 pin.	Secondary	—
CS1	O	Reference capacitor connection pin of Channel 1. This pin is used as the secondary function of the P45 pin.	Secondary	—
RS1	O	Reference resistor connection pin of Channel 1. This pin is used as the secondary function of the P46 pin.	Secondary	—
RT1	O	Resistor sensor connection pin for measurement of Channel 1. This pin is used as the secondary function of the P47 pin.	Secondary	—
Successive approximation type A/D converter				
AV _{SS}	—	Negative power supply pin for successive approximation type A/D converter.	—	—
AV _{DD}	—	Positive power supply pin for successive approximation type A/D converter.	—	—
V _{REF}	—	Reference power supply pin for successive approximation type A/D converter.	—	—
AIN0	I	Channel 0 analog input for successive approximation type A/D converter.	—	—
AIN1	I	Channel 1 analog input for successive approximation type A/D converter.	—	—
LCD drive signal				
COM0-3	O	Common output pins.	—	—
SEG0-35	O	Segment output pins.	—	—
SEG36-43	O	Segment output pin. These pins are for the ML610Q412, but are not provided in the ML610Q411 and ML610Q415.	—	—
LCD driver power supply				
V _{L1}	—	Power supply pins for LCD bias (internally generated). Capacitors Ca, Cb, and Cc (see measuring circuit 1) are connected between V _{SS} and V _{L1} , V _{L2} , and V _{L3} , respectively.	—	—
V _{L2}	—		—	—
V _{L3}	—		—	—
C1	—	Power supply pins for LCD bias (internally generated). Capacitors C12 is connected between C1 and C2.	—	—
C2	—		—	—
For testing				
TEST	I/O	Input/output pin for testing. A pull-down resistor is internally connected.	—	—
Power supply				
V _{SS}	—	Negative power supply pin.	—	—
V _{DD}	—	Positive power supply pin for I/O, internal regulator, battery low detector, and power-on reset.	—	—
V _{DDL}	—	Positive power supply pin (internally generated) for internal logic. Capacitors CL0 and CL1 (see measuring circuit 1) are connected between this pin and V _{SS} .	—	—
V _{DDX}	—	Positive power supply pin (internally generated) for low-speed oscillation. When using ML610Q411 and ML610Q412, connect capacitor Cx (see measuring circuit 1) between this pin and V _{SS} . Connect this pin to V _{SS} directly when using ML610Q415.	—	—
V _{PP}	—	Power supply pin for programming Flash ROM. A pull-down resistor is internally connected.	—	—

TERMINATION OF UNUSED PINS

Table 3 shows methods of terminating the unused pins.

Table 3 Termination of Unused Pins

Pin	Recommended pin termination
V _{FP}	Open
AV _{DD}	V _{SS}
AV _{SS}	V _{SS}
V _{DDX}	V _{SS} (ML610Q415)
V _{REF}	V _{SS}
XT0	V _{SS} (ML610Q415)
XT1	Open (ML610Q415)
AIN0, AIN1	Open
V _{L1} , V _{L2} , V _{L3}	Open
C1, C2	Open
RESET_N	Open
TEST	Open
NMI	Open
P00 to P03	V _{DD} or V _{SS}
P10 to P11	V _{DD}
P20 to P22	Open
P30 to P35	Open
P40 to P47	Open
PA0 to PA7	Open
COM0 to 3	Open
SEG0 to 43	Open

Note:

It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

ELECTRICAL CHARACTERISTICS

(To be reviewed after ES evaluation. The wide temperature product P version will be determined in revised data sheet)

ABSOLUTE MAXIMUM RATINGS(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V _{DD}	Ta = 25°C	-0.3 to +4.6	V
Power supply voltage 2	AV _{DD}	Ta = 25°C	-0.3 to +4.6	V
Power supply voltage 3	V _{FP}	Ta = 25°C	-0.3 to +9.5	V
Power supply voltage 4	V _{DDL}	Ta = 25°C	-0.3 to +3.6	V
Power supply voltage 5	V _{DDX}	Ta = 25°C	-0.3 to +3.6	V
Power supply voltage 6	V _{L1}	Ta = 25°C	-0.3 to +1.75	V
Power supply voltage 7	V _{L2}	Ta = 25°C	-0.3 to +3.5	V
Power supply voltage 8	V _{L3}	Ta = 25°C	-0.3 to +5.25	V
Input voltage	V _{IN}	Ta = 25°C	-0.3 to V _{DD} +0.3	V
Output voltage	V _{OUT}	Ta = 25°C	-0.3 to V _{DD} +0.3	V
Output current 1	I _{OUT1}	Port3-A, Ta = 25°C	-12 to +11	mA
Output current 2	I _{OUT2}	Port2, Ta = 25°C	-12 to +20	mA
Power dissipation	PD	Ta = 25°C	1.25	W
Storage temperature	T _{STG}	—	-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T _{OP}	ML610Q411, ML610Q412, ML610Q415	-20 to +70	°C
		ML610Q411, ML610Q412	-40 to +85	
Operating voltage	V _{DD}	—	1.1 to 3.6	V
	AV _{DD}	—	2.2 to 3.6	
Operating frequency (CPU)	f _{OP}	V _{DD} = 1.1 to 3.6V	30k to 36k	Hz
		V _{DD} = 1.3 to 3.6V	30k to 625k	
Low-speed crystal oscillation frequency	f _{XTL}	ML610Q411/ML610Q412	32.768k	Hz
Low-speed crystal oscillation external capacitor	C _{DL}	—	0 to 12	pF
	C _{GL}	—	0 to 12	
Capacitor externally connected to V _{DDL} pin	C _{LD}	—	1.0±30%	μF
	C _{L1}	—	0.1±30%	
Capacitor externally connected to V _{DDX} pin	C _X	ML610Q411/ML610Q412	0.1±30%	μF
Capacitors externally connected to V _{L1, 2, 3} pins	C _{1, 2, 3}	—	1.0±30%	μF
Capacitors externally connected across C1 and C2 pins	C ₁₂	—	1.0±30%	μF

OPERATING CONDITIONS OF FLASH ROM(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T _{OP}	At write/erase	0 to +40	°C
Operating voltage	V _{DD}	At write/erase ^{*1}	2.75 to 3.6	V
	V _{DDL}	At write/erase ^{*1}	2.5 to 2.75	
	V _{PP}	At write/erase ^{*1}	7.7 to 8.3	
Write cycles	C _{EP}	—	80	cycles
Data retention	Y _{DR}	—	10	years

*1: Those voltages must be supplied to V_{DDL} pin and V_{PP} pin when programming and erasing Flash ROM.

DC CHARACTERISTICS (1/5)(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = -20 to +70°C, unless otherwise specified) (1/5)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
500kHz RC oscillation frequency	f _{RC}	V _{DD} = 1.3 to 3.6V	Ta = 25°C	Typ. -10%	500	Typ. +10%	kHz
			Ta = -20 to +70°C	Typ. -25%	500	Typ. +25%	
Low-speed crystal oscillation start time ^{*2}	T _{XTL}	—	—	0.3	2	s	1
500kHz RC oscillation start time	T _{RC}	—	—	50	500	μs	
Low-speed oscillation stop detect time ^{*1}	T _{STOP}	—	0.2	3	20	ms	
Reset pulse width	P _{RST}	—	200	—	—	μs	
Reset noise elimination pulse width	P _{NRST}	—	—	—	0.3		
Power-on reset activation power rise time	T _{POR}	—	—	—	10	ms	

*1: When low-speed crystal oscillation stops for a duration more than the low-speed oscillation stop detect time, the system is reset to shift to system reset mode.

*2: Use 32.768KHz Crystal Oscillator C-001R (Epson Toyocom) with capacitance C_{GL}/C_{DL} = 0pF.

DC CHARACTERISTICS (2/5)(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = -20 to +70°C, unless otherwise specified) (2/5)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit	
			Min.	Typ.	Max.			
V _{L1} voltage	V _{L1}	V _{DD} = 3.0V, T _j = 25°C	CN4-0 = 00H	0.89	0.94	0.99	V	1
			CN4-0 = 01H	0.91	0.96	1.01		
			CN4-0 = 02H	0.93	0.98	1.03		
			CN4-0 = 03H	0.95	1.00	1.05		
			CN4-0 = 04H	0.97	1.02	1.07		
			CN4-0 = 05H	0.99	1.04	1.09		
			CN4-0 = 06H	1.01	1.06	1.11		
			CN4-0 = 07H	1.03	1.08	1.13		
			CN4-0 = 08H	1.05	1.10	1.15		
			CN4-0 = 09H	1.07	1.12	1.17		
			CN4-0 = 0AH	1.09	1.14	1.19		
			CN4-0 = 0BH	1.11	1.16	1.21		
			CN4-0 = 0CH	1.13	1.18	1.23		
			CN4-0 = 0DH	1.15	1.20	1.25		
			CN4-0 = 0EH	1.17	1.22	1.27		
			CN4-0 = 0FH	1.19	1.24	1.29		
			CN4-0 = 10H	1.21	1.26	1.31		
			CN4-0 = 11H	1.23	1.28	1.33		
			CN4-0 = 12H	1.25	1.30	1.35		
			CN4-0 = 13H	1.27	1.32	1.37		
			CN4-0 = 14H ^{*1}	1.29	1.34	1.39		
			CN4-0 = 15H ^{*1}	1.31	1.36	1.41		
			CN4-0 = 16H ^{*1}	1.33	1.38	1.43		
			CN4-0 = 17H ^{*1}	1.35	1.40	1.45		
CN4-0 = 18H ^{*1}	1.37	1.42	1.47					
CN4-0 = 19H ^{*1}	1.39	1.44	1.49					
CN4-0 = 1AH ^{*1}	1.41	1.46	1.51					
CN4-0 = 1BH ^{*1}	1.43	1.48	1.53					
CN4-0 = 1CH ^{*1}	1.45	1.50	1.55					
CN4-0 = 1DH ^{*1}	1.47	1.52	1.57					
CN4-0 = 1EH ^{*1}	1.49	1.54	1.59					
CN4-0 = 1FH ^{*1}	1.51	1.56	1.61					
V _{L1} temperature deviation	ΔV _{L1}	V _{DD} = 3.0V	—	-1.5	—	mV/°C		
V _{L1} voltage dependency	ΔV _{L1}	V _{DD} = 1.3 to 3.6V	—	5	20	mV/V		
V _{L2} voltage	V _{L2}	V _{DD} = 3.0V, T _j = 25°C 300kΩ load (V _{L3} -V _{SS})	Typ. -10%	V _{L1} ×2	Typ. +4%	V		
V _{L3} voltage	V _{L3}		Typ. -10%	V _{L1} ×3	Typ. +4%			
LCD bias voltage generation time	T _{BIAS}	—	—	—	600	ms		

DC CHARACTERISTICS (3/5)(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = -20 to +70°C, unless otherwise specified) (3/5)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit		
			Min.	Typ.	Max.				
BLD threshold voltage	V _{BLD}	V _{DD} = 1.35 to 3.6V	Typ. -2%		Typ. +2%	V			
								LD2-0 = 0H	1.35
								LD2-0 = 1H	1.4
								LD2-0 = 2H	1.45
								LD2-0 = 3H	1.5
								LD2-0 = 4H	1.6
								LD2-0 = 5H	1.7
								LD2-0 = 6H	1.8
								LD2-0 = 7H	1.9
								LD2-0 = 8H	2.0
								LD2-0 = 9H	2.1
								LD2-0 = 0AH	2.2
								LD2-0 = 0BH	2.3
								LD2-0 = 0CH	2.4
LD2-0 = 0DH	2.5								
LD2-0 = 0EH	2.7								
LD2-0 = 0FH	2.9								
BLD threshold voltage temperature deviation	ΔV _{BLD}	V _{DD} = 1.35 to 3.6V	—	0	—	%/°C			
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed RC500kHz oscillation: stopped.	—	0.15	2.5	μA			
Supply current 2-1* ⁵	IDD2-1	CPU: In HALT state (LTBC and WDT are Operating. Low speed oscillation stop detector is Stopped). ^{*3*4} High-speed 500kHz oscillation: Stopped. LCD and BIAS circuits: Stopped.	—	0.5	3.5	μA	1		
Supply current 2-2* ⁶	IDD2-2	CPU: In HALT state (LTBC and WDT are Operating. Low speed oscillation stop detector is Stopped). ^{*3*4} High-speed oscillation: Oscillating. LCD and BIAS circuits: Stopped.	—	5.5	16	μA			
Supply current 3-1* ⁵	IDD3-1	CPU: In HALT state (LTBC and WDT are Operating. Low speed oscillation stop detector is Stopped). ^{*3} High-speed 500kHz oscillation: Stopped. LCD and BIAS circuits: Operating. ^{*2}	—	1.28	11	μA			
Supply current 3-2* ⁶	IDD3-2	CPU: In HALT state (LTBC and WDT are Operating. Low speed oscillation stop detector is Stopped). ^{*3} High-speed 500kHz oscillation: Oscillating. LCD and BIAS circuits: Operating. ^{*2}	—	6.28	23.5	μA			
Supply current 4	IDD4	CPU: In 32.768kHz operating state. ^{*1*3} High-speed 500kHz oscillation: Stopped. LCD and BIAS circuits: Operating. ^{*2}	—	2	12	μA			
Supply current 5	IDD5	CPU: In RC 500kHz operating state. LCD and BIAS circuits: Operating. ^{*2}	—	82	100	μA			
Supply current 6	IDD6	CPU: In RC 500kHz operating state. ^{*2} LCD and BIAS circuits: Operating. ^{*2} A/D: In operating state. V _{DD} = AV _{DD} = 3.0V	—	0.96	1.6	mA			

*1: When the CPU operating rate is 10% (90%: In HALT state).

*2: All SEGs: off waveform, No LCD panel load, 1/3 bias, 1/3 duty, Frame frequency: Approx. 64 Hz, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)

*3: Use 32.768KHz Crystal Oscillator C-001R (Epson Toyocom) with capacitance $C_{GL}/C_{DL} = 0pF$.

*4: Significant bits of BLKCON0~BLKCON4 registers are all "1".

*5: ML610Q411 and ML610Q412

*6: ML610Q415

DC CHARACTERISTICS (4/5)

($V_{DD} = 1.1$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^{\circ}C$, unless otherwise specified) (4/5)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit	
			Min.	Typ.	Max.			
Output voltage 1 (P20-P22) (P30-P36) (P40-P47) (PB0-PB7) ^{*1}	VOH1	IOH1 = -0.5mA, $V_{DD} = 1.8$ to $3.6V$	V_{DD} -0.5	—	—	V	2	
		IOH1 = -0.1mA, $V_{DD} = 1.3$ to $3.6V$	V_{DD} -0.3	—	—			
		IOH1 = -0.03mA, $V_{DD} = 1.1$ to $3.6V$	V_{DD} -0.3	—	—			
	VOL1	IOL1 = +0.5mA, $V_{DD} = 1.8$ to $3.6V$	—	—	0.5			
		IOL1 = +0.1mA, $V_{DD} = 1.3$ to $3.6V$	—	—	0.5			
		IOL1 = +0.03mA, $V_{DD} = 1.1$ to $3.6V$	—	—	0.3			
Output voltage 2 (P20-P22)	VOL2	IOL2 = +5mA, $V_{DD} = 1.8$ to $3.6V$ (when LED drive mode is selected)	—	—	0.5	V	2	
Output voltage 3 (P40-P41)	VOL3	IOL3 = +3mA, $V_{DD} = 2.0$ to $3.6V$ (when I ² C mode is selected)	—	—	0.4			
Output voltage 4 (COM0-3) (SEG0-35) ^{*1} (SEG0-43) ^{*2}	VOH4	IOH4 = -0.2mA, $V_{L1} = 1.2V$	V_{L4} -0.2	—	—			
	VOMH4	IOMH4 = +0.2mA, $V_{L1} = 1.2V$	—	—	V_{L3} +0.2			
	VOMH4S	IOMH4S = -0.2mA, $V_{L1} = 1.2V$	V_{L3} -0.2	—	—			
	VOM4	IOM4 = +0.2mA, $V_{L1} = 1.2V$	—	—	V_{L2} +0.2			
	VOM4S	IOM4S = -0.2mA, $V_{L1} = 1.2V$	V_{L2} -0.2	—	—			
	VOML4	IOML4 = +0.2mA, $V_{L1} = 1.2V$	—	—	V_{L1} +0.2			
	VOML4S	IOML4S = -0.2mA, $V_{L1} = 1.2V$	V_{L4} -0.2	—	—			
	VOL4	IOL4 = +0.2mA, $V_{L1} = 1.2V$	—	—	0.2			
Output leakage (P20-P22) (P30-P35) (P40-P47) (PA0-PA7) ^{*1}	IOOH	VOH = V_{DD} (in high-impedance state)	—	—	1	μA	3	
	IOOL	VOL = V_{SS} (in high-impedance state)	-1	—	—			
Input current 1 (RESET_N)	IIH1	$V_{IH1} = V_{DD}$		0	—	1	μA	4
	IIL1	$V_{IL1} = V_{SS}$	$V_{DD} = 1.3$ to $3.6V$	-600	-300	-10		
			$V_{DD} = 1.1$ to $3.6V$	-600	-300	-2		
Input current 1 (TEST)	IIH1	$V_{IH1} = V_{DD}$	$V_{DD} = 1.3$ to $3.6V$	10	300	600		
			$V_{DD} = 1.1$ to $3.6V$	2	300	600		
	IIL1	$V_{IL1} = V_{SS}$		-1	—	—		
Input current 2 (NMI) (P00-P03) (P10-P11)	IIH2	$V_{IH2} = V_{DD}$ (when pulled-down)	$V_{DD} = 1.3$ to $3.6V$	0.2	30	200		
			$V_{DD} = 1.1$ to $3.6V$	0.01	30	200		
	IIL2	$V_{IL2} = V_{SS}$ (when pulled-up)	$V_{DD} = 1.3$ to $3.6V$	-200	-30	-0.2		
			$V_{DD} = 1.1$ to $3.6V$	-200	-30	-0.01		

(P30-P35) (P40-P47) (PA0-PA7) ^{*1}	I1H2Z	VIH2 = V _{DD} (in high-impedance state)	—	—	1		
	I1L2Z	VIL2 = V _{SS} (in high-impedance state)	-1	—	—		

*1: ML610Q411 and ML610Q415

*2: ML610Q412

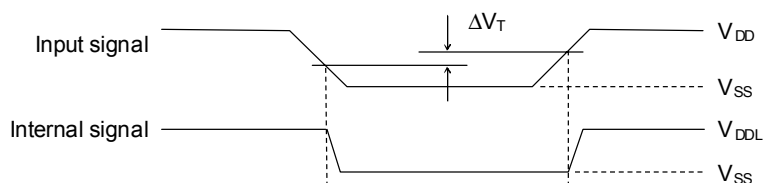
DC CHARACTERISTICS (5/5)

(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = -20 to +70°C, unless otherwise specified) (5/5)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N) (TEST) (NMI) (P00-P03) (P10-P11) (P31-P35) (P40-P43) (P45-P47) (PA0-PA7) ^{*1}	VIH1	V _{DD} = 1.3 to 3.6V	0.7 ×V _{DD}	—	V _{DD}	V	5
		V _{DD} = 1.1 to 3.6V	0.7 ×V _{DD}	—	V _{DD}		
	VIL1	V _{DD} = 1.3 to 3.6V	0	—	0.3 ×V _{DD}		
		V _{DD} = 1.1 to 3.6V	0	—	0.2 ×V _{DD}		
Hysteresis width (RESET_N) (TEST_N) (NMI) (P00-P03) (P10-P11) (P31-P35) (P40-P43) (P45-P47) (PA0-PA7) ^{*1}	ΔVT	V _{DD} = 2.0 to 3.6V	0.05 ×V _{DD}	0.18 ×V _{DD}	0.4 ×V _{DD}	V	5
		V _{DD} = 1.1 to 3.6V	0.02 ×V _{DD}	0.18 ×V _{DD}	0.4 ×V _{DD}		
Input voltage 2 (P30, P44)	VIH2	—	0.7 ×V _{DD}	—	V _{DD}	pF	—
	VIL2	—	0	—	0.3 ×V _{DD}		
Input pin capacitance (NMI) (P00-P03) (P10-P11) (P30-P35) (P40-P47) (PA0-PA7) ^{*1}	CIN	f = 10kHz V _{rms} = 50mV Ta = 25°C	—	—	5	pF	—

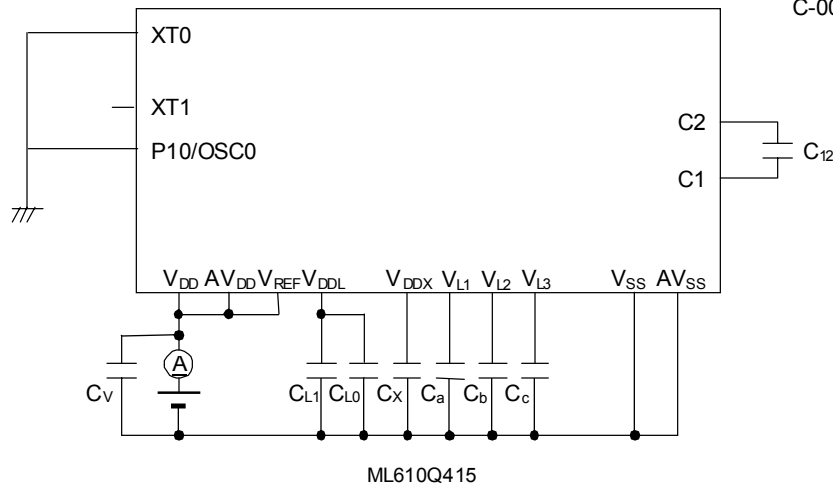
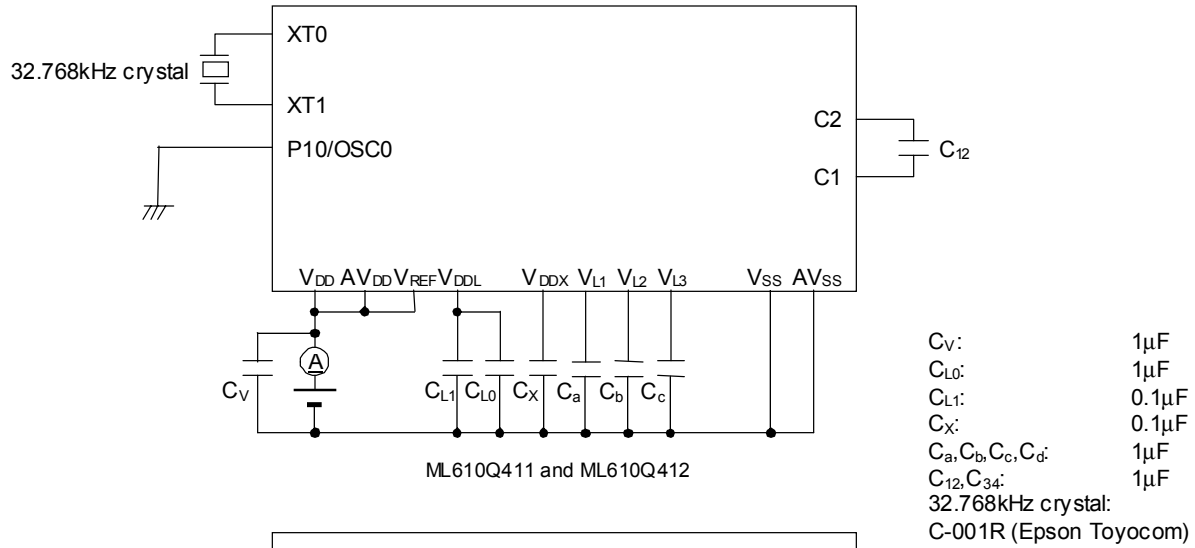
*1: ML610Q411 and ML610Q415

HYSTERESIS WIDTH

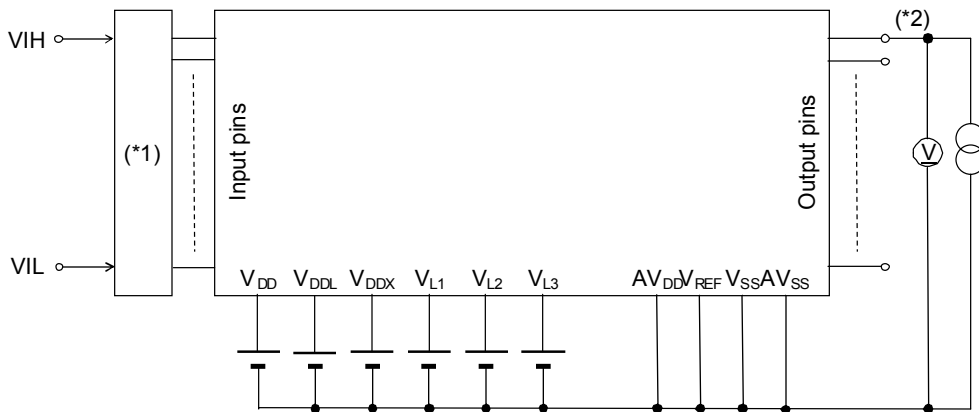


MEASURING CIRCUITS

MEASURING CIRCUIT 1 (TBD)

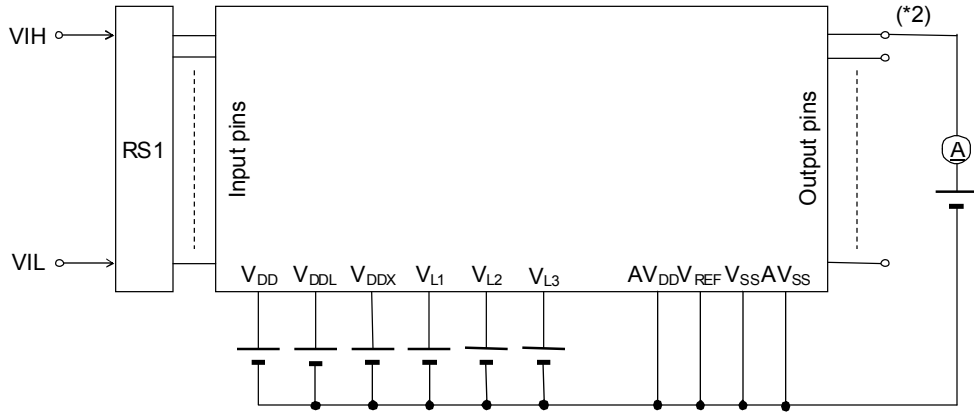


MEASURING CIRCUIT 2 (TBD)



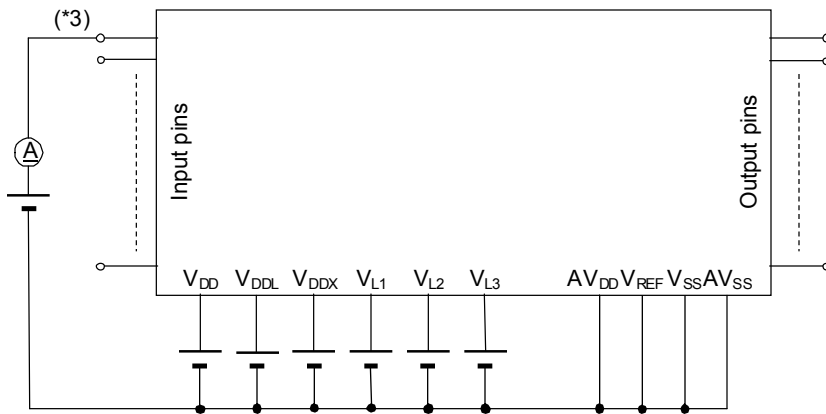
(*1) Input logic circuit to determine the specified measuring conditions.
 (*2) Measured at the specified output pins.

MEASURING CIRCUIT 3 (TBD)



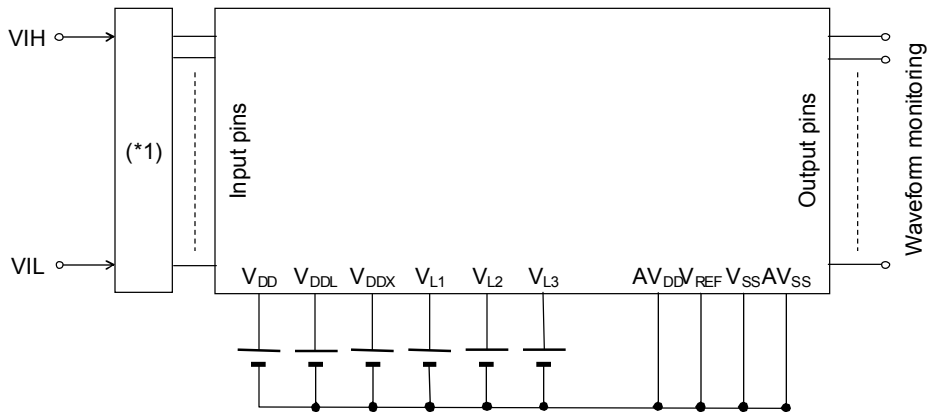
*1: Input logic circuit to determine the specified measuring conditions.
 *2: Measured at the specified output pins.

MEASURING CIRCUIT 4 (TBD)



*3: Measured at the specified output pins.

MEASURING CIRCUIT 5 (TBD)

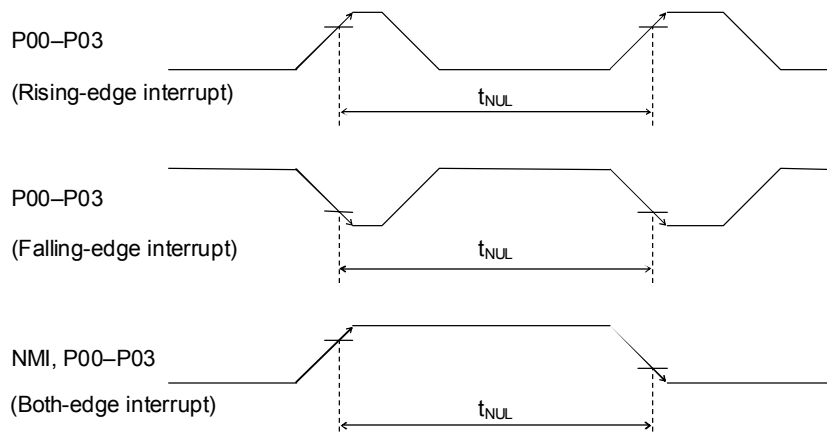


*1: Input logic circuit to determine the specified measuring conditions.

AC CHARACTERISTICS (External Interrupt)

($V_{DD} = 1.1$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation System clock: 32.768kHz	76.8	—	106.8	μs

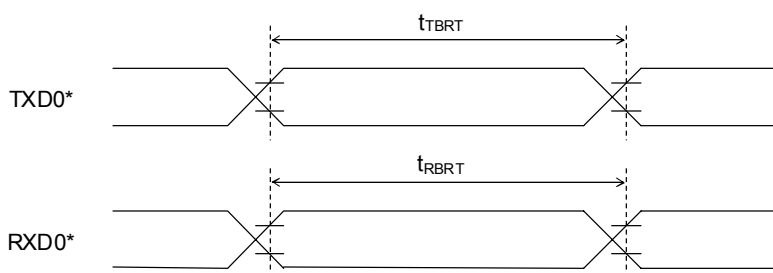


AC CHARACTERISTICS (Serial Port)

($V_{DD} = 1.3$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Transmit baud rate	t_{TBRT}	—	—	BRT* ¹	—	s
Receive baud rate	t_{RBRT}	—	BRT* ¹ -3%	BRT* ¹	BRT* ¹ +3%	s

*1: Baud rate period (including the error of the clock frequency selected) set with the serial port baud rate register (SIOBRTL,H) and the serial port mode register 0 (SIOMOD0).



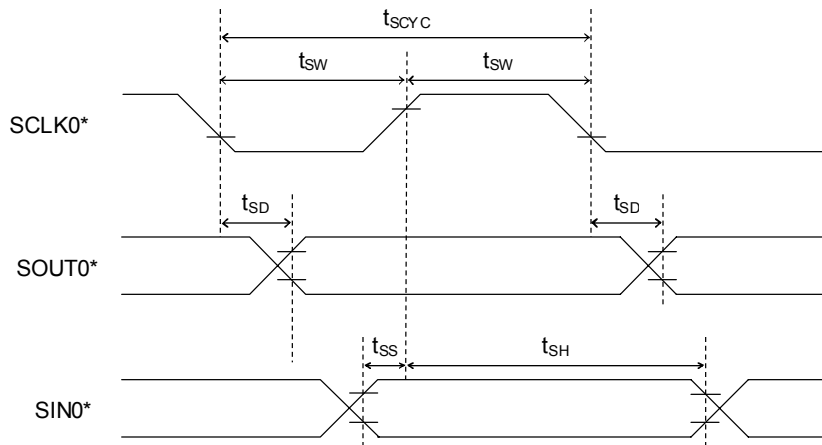
*: Indicates the secondary function of the port.

AC CHARACTERISTICS (Synchronous Serial Port)

($V_{DD} = 1.3$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLK input cycle (slave mode)	t_{SCYC}	When high-speed oscillation is not active	10	—	—	μs
SCLK output cycle (master mode)	t_{SCYC}	—	—	$SCLK^{*1}$	—	s
SCLK input pulse width (slave mode)	t_{SW}	When high-speed oscillation is not active	4	—	—	μs
SCLK output pulse width (master mode)	t_{SW}	—	$SCLK^{*1} \times 0.4$	$SCLK^{*1} \times 0.5$	$SCLK^{*1} \times 0.6$	s
SOUT output delay time (slave mode)	t_{SD}	—	—	—	180	ns
SOUT output delay time (master mode)	t_{SD}	—	—	—	80	ns
SIN input setup time (slave mode)	t_{SS}	—	80	—	—	ns
SIN input setup time (master mode)	t_{SS}	—	180	—	—	ns
SIN input hold time	t_{SH}	—	80	—	—	ns

*1: Clock period selected with S0CK3-0 of the serial port 0 mode register (SIO0MOD1)

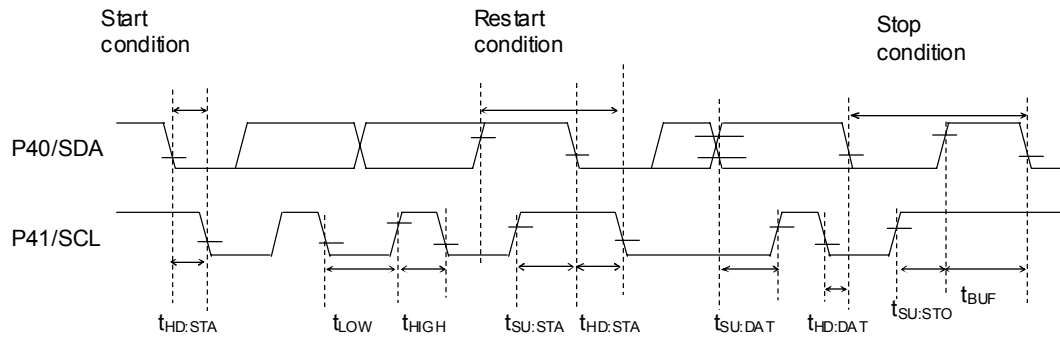


*: Indicates the secondary function of the port.

AC CHARACTERISTICS (I²C Bus Interface: Standard Mode)

(V_{DD} = 1.8 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = -20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f _{SCL}	—	—	50	—	kHz
SCL hold time (start/restart condition)	t _{HD:STA}	—	4.0	—	—	μs
SCL "L" level time	t _{LOW}	—	4.7	—	—	μs
SCL "H" level time	t _{HIGH}	—	4.0	—	—	μs
SCL setup time (restart condition)	t _{SU:STA}	—	4.7	—	—	μs
SDA hold time	t _{HD:DAT}	—	0	—	3.45	μs
SDA setup time	t _{SU:DAT}	—	0.25	—	—	μs
SDA setup time (stop condition)	t _{SU:STO}	—	4.0	—	—	μs
Bus-free time	t _{BUF}	—	4.7	—	—	μs



AC CHARACTERISTICS (RC Oscillation A/D Converter)

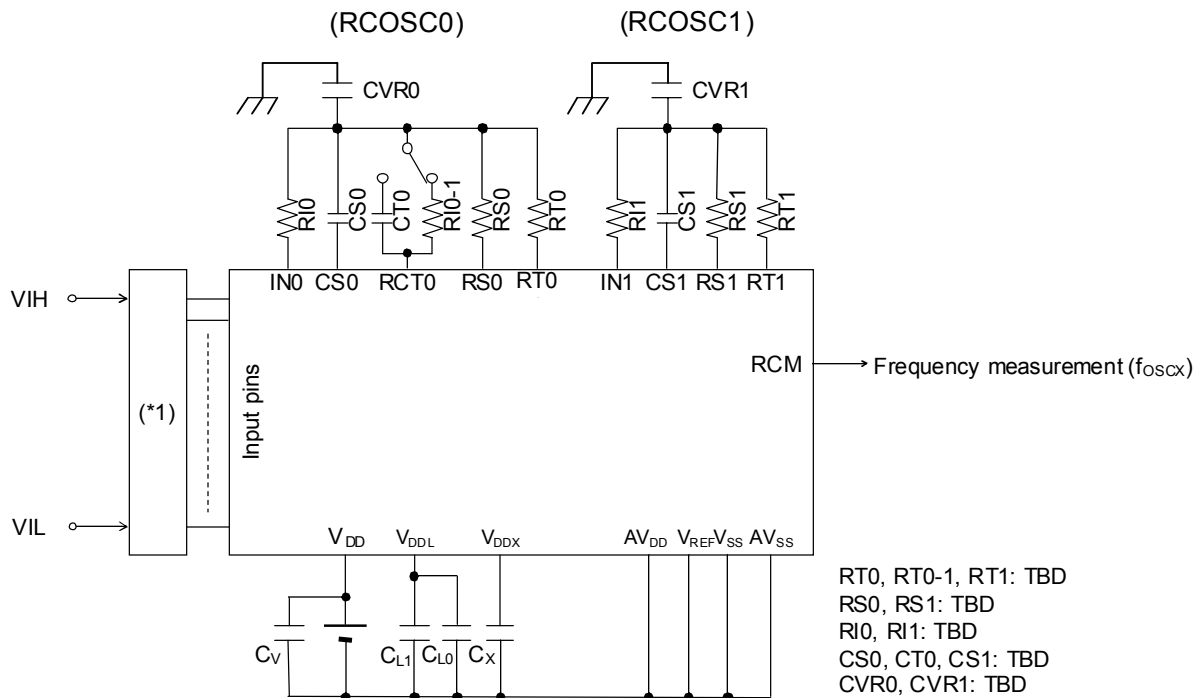
(V_{DD} = 1.3 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = -20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Resistors for oscillation	RS0, RS1, RT0, RT0-1, RT1	CS0, CT0, CS1 ≥ 740pF	2	—	—	kΩ
Input current limit resistors	RI0, RI1	—	1	10	—	kΩ
Oscillation frequency VDD = 1.5V	f _{OSC1}	Resistor for oscillation = 2Ω	TBD	TBD	TBD	kHz
	f _{OSC2}	Resistor for oscillation = 1kΩ	TBD	TBD	TBD	kHz
	f _{OSC3}	Resistor for oscillation = 20kΩ	TBD	TBD	TBD	kHz
RS to RT oscillation frequency ratio *1 VDD = 1.5V	Kf1	RT0, RT0-1, RT1 = 2 kHz	TBD	TBD	TBD	—
	Kf2	RT0, RT0-1, RT1 = 10 kHz	TBD	TBD	TBD	—
	Kf3	RT0, RT0-1, RT1 = 200 kHz	TBD	TBD	TBD	—
Oscillation frequency VDD = 3.0V	f _{OSC1}	Resistor for oscillation = 2Ω	TBD	TBD	TBD	kHz
	f _{OSC2}	Resistor for oscillation = 1kΩ	TBD	TBD	TBD	kHz
	f _{OSC3}	Resistor for oscillation = 20kΩ	TBD	TBD	TBD	kHz
RS to RT oscillation frequency ratio *1 VDD = 3.0V	Kf1	RT0, RT0-1, RT1 = 2 kHz	TBD	TBD	TBD	—
	Kf2	RT0, RT0-1, RT1 = 10 kHz	TBD	TBD	TBD	—
	Kf3	RT0, RT0-1, RT1 = 200 kHz	TBD	TBD	TBD	—

*1: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{oscx}(RT0-CS0 \text{ oscillation})}{f_{oscx}(RS0-CS0 \text{ oscillation})}, \quad \frac{f_{oscx}(RT0-1-CS0 \text{ oscillation})}{f_{oscx}(RS0-CS0 \text{ oscillation})}, \quad \frac{f_{oscx}(RT1-CS1 \text{ oscillation})}{f_{oscx}(RS1-CS1 \text{ oscillation})}$$

(x = 1, 2, 3)



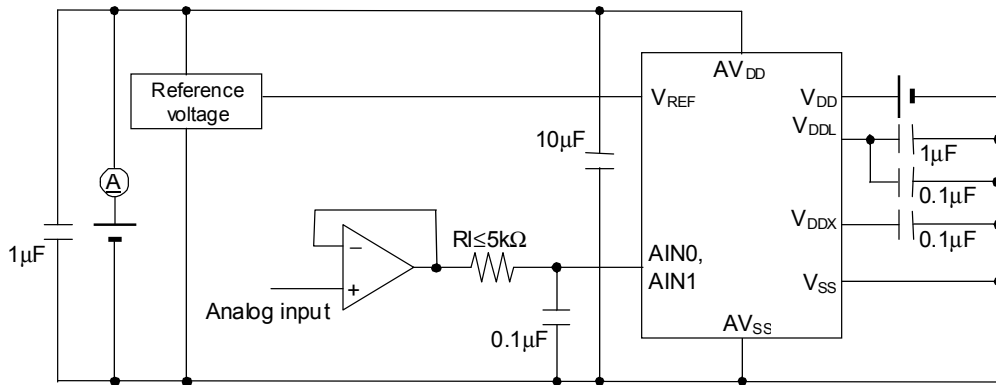
*1: Input logic circuit to determine the specified measuring conditions.

Electrical Characteristics of Successive Approximation Type A/D Converter

($V_{DD} = 1.8$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^{\circ}C$, unless otherwise specified)

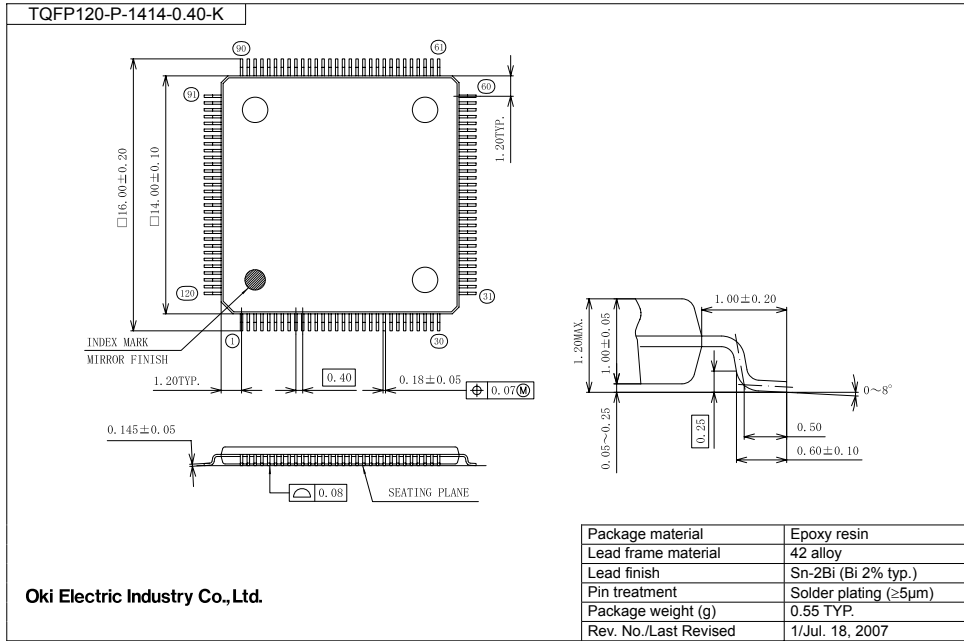
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Resolution	n	—	—	—	12	bit
Integral non-linearity error	IDL	$2.7V \leq V_{REF} \leq 3.6V$	-4	—	+4	LSB
		$2.2V \leq V_{REF} \leq 2.7V$	-6	—	+6	
Differential non-linearity error	DNL	$2.7V \leq V_{REF} \leq 3.6V$	-3	—	+3	
		$2.2V \leq V_{REF} \leq 2.7V$	-5	—	+5	
Zero-scale error	V_{OFF}	—	-6	—	+6	
Full-scale error	FSE	—	-6	—	+6	
Reference voltage	V_{REF}	—	2.2	—	AV_{DD}	V
Conversion time	t_{CONV}	—	—	23	—	ϕ/CH

ϕ : Period of high-speed clock (HSCLK)



Package Dimensions

(Unit mm)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL610Q411-01	Jul.08,2008	–	–	Preliminary edition 1
PEDL610Q411-02	Aug.06,2008	–	2, 3, 6, 9, 12, 16, 17, 18, 19, 21, 22, 26, 27	Add ML610Q415 (No crystal oscillation version)
		1	1	Correct the number of maskable interrupt
		2	2	Add SA-A/D converter conversion time Add description for Timer
		4, 5	4, 5	Change PB0-PB7 to PA0-PA7 Correct the number of interrupt in timer block
		–	6	Add ML610Q415 block diagram
		7	10	Add ML610Q411 pad layout. Update chip size, number of pad and pad aperture.
		8	11	Add ML610Q412 pad layout. Update chip size, number of pad and pad aperture.
		–	12	Add ML610Q415 pad layout
		13	17	Change pin layout of Port3 (RCADC ch0).
		13, 15, 18	17, 19, 22	Change PB0-PB7 to PA0-PA7.
		17, 18	21, 22	Add description for VDDX pin
		16, 18	19, 22	Add description for XT0 and XT1 pin.
		18	22	Delete V _{L4} , C3, and C4.
		19	23	Delete Power Supply 9 (V _{L4}). Delete C ₃₄ . Change the spec of Power dissipation.
		20	24	Change reset pulse width and reset noise elimination pulse width.
		21	25	Change LCD bias voltage generation time.
		22	26	Correct condition of current consumption.
23	27	Change PB0-PB7 to PA0-PA7		
25	29	Add measurement circuit for Q415.		
30	34	Change pin layout of Port3 (RCADC ch0).		
PEDL610Q411-03	Sep.15,2008	1, 2, 3	1, 2, 3	Add difference between ML610Q411/Q412 and ML610Q415.
		2	2	Correct I2C clock frequency 100k bps to 50k bps.
		4, 6	4	Combine block diagram ML610Q415 and ML610Q411.
		7 to 9	6, 7	Add PKG pin-layout.
		10 to 12	8, 9	Add Chip pin-layout.
		13 to 15	10, 11	Add pad coordinates.
		16 to 18	12 to 14	Add pin numbers on the pin table.
		19	15	Add a note for unused pin XT1 on ML610Q415.
		23	19	Split the condition for operating temperature. Change the max. operating frequency 650kHz to 625kHz.
		24	20	Change VDD at writing/erasing Flash ROM 2.7V to 2.75V.
		25	21	Change LCD bias voltage generating time 1200ms to 600ms.
		27	23	Correct a typo in condition for output voltage 4, (COM0 to 23) → (COM0 to 3).
33	29	Change the spec for I2C clock frequency fSCL, “0 to 100kHz” to “typ.50kHz”.		
34	30	Change RC-ADC recommended circuit. Change the specs to TBD(To Be Determined).		

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.
2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.
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