ML610404/ML610405/ML610406 Preliminary

8-bit Microcontroller with a Built-in LCD driver

GENERAL DESCRIPTION

ML610404/ML610405/ML610406 is a high-performance 8-bit CMOS microcontroller into which peripheral circuits, such as synchronous serial port, UART, melody driver, RC oscillation type A/D converter, and LCD driver, are incorporated around OKI Semiconductor-original 8-bit CPU nX-U8/100. ML610404/ML610405/ML610406 operates in both high/low-speed mode and power-saving mode, it is most suitable for battery operated products.
The short TAT are entertained by offering MTP version ML610Q407(P)/ML610Q408(P)/ML610Q409(P). ML610404P/ ML610405P/ML610406P support industrial temperature -40°C to +85°C, are added to the product lineup.

FEATURES

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction system: 16-bit instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - Minimum instruction execution time
    30.5 μs (@32.768 kHz system clock)
    2μs (@500kHz system clock)
    0.5μs(@2MHz system clock)

- Internal memory
  - ML610404/5/6 :
    Internal 8KByte Mask ROM (4K×16 bits) (including unusable 256 Byte TEST area)
    Internal 256Byte Data RAM (256×8 bits)

- Interrupt controller
  - 1 non-maskable interrupt sources
    Internal source: 1 (Watch dog timer)
  - 27 maskable interrupt sources
    Internal sources: 14 (SSIO0, SSIO1, Timer0, Timer1, Timer2, Timer3, UART0, Melody0, RC-A/D converter, PWM0, TBC128Hz, TBC32Hz, TBC16Hz, TBC2Hz)
    External sources: 13 (P00, P01, P02, P03, P04, P50, P51, P52, P53, P54, P55, P56, P57)
    (One interrupt request is generated from P50 to P57 interrupt sources.)

- Time base counter
  - Low-speed time base counter ×1 channel
    Frequency compensation (Compensation range: Approx. –488ppm to +488ppm. Compensation accuracy: Approx. 0.48ppm)
  - High-speed time base counter ×1 channel

- Watchdog timer
  - Non-maskable interrupt and reset
  - Free running
  - Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s)

- Timers
  - 8 bits × 4 channels (Timer0-3: 16-bit x 2 configuration available by using Timer0-1 or Timer2-3)
  - Clock frequency measurement mode (in one channel of 16-bit configuration using Timer2-3)

- Capture
  - Time base capture × 2 channels (4096 Hz to 32 Hz)

- PWM
  - Resolution 16 bits × 1 channel

- Synchronous serial port
  - Master/slave selectable × 2 channel
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable

- UART
  - TXD/RXD × 1 channel
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - Built-in baud rate generator

- Melody driver
  - Scale: 29 types (Melody sound frequency: 508 Hz to 32.768 kHz)
  - Tone length: 63 types
  - Tempo: 15 types
  - Buzzer output mode (4 output modes, 8 frequencies, 16 duty levels)

- RC oscillation type A/D converter
  - 16-bit counter
  - Time division × 2 channels

- General-purpose ports
  - Input-only port × 5 channels (including secondary functions)
  - Output-only port
    ML610404: × 12 channels (including secondary functions)
    ML610405: × 8 channels (including secondary functions)
    ML610406: × 4 channels (including secondary functions)
  - Input/output port × 22 channels (including secondary functions)

- LCD driver
  - The number of segments
    ML610404: 105 dots max. (21seg×5com, 22seg×4com, 23seg×3com, and 24seg×2com selectable)
    ML610405: 125 dots max. (25seg×5com, 26seg×4com, 27seg×3com, and 28seg×2com selectable)
    ML610406: 145 dots max. (29seg×5com, 30seg×4com, 31seg×3com, and 32seg×2com selectable)
  - 1/1 to 1/5 duty

- 1/2, 1/3 bias (built-in bias generation circuit)
- Frame frequency selecable: approx. 64Hz, 73Hz, 85Hz, and 102Hz
- Bias voltage multiplying clock selectable (8 types)
- LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable
- Programmable display allocation function

- Reset
  - Reset through the RESET_N pin
  - Power-on reset generation when powered on
  - Reset when oscillation stop of the low-speed clock is detected
  - Reset by the watchdog timer (WDT) overflow

- Clock
  - Low-speed clock: Crystal oscillation (32.768 kHz)
    (This LSI can not guarantee the operation withoug low-speed crystal oscillation clock)
  - High-speed clock: Built-in RC oscillation (500 kHz, 2MHz)

- Power management
  - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - High-speed Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, 1/8 of the oscillation clock)
  - Block Control Function: Resets and completely turns circuits of unused peripherals off.

- Shipment
  - Chip
    ML610404P-xxxWA
    ML610405P-xxxWA
    ML610406P-xxxWA
  - 80-pin plastic TQFP
    ML610404P-xxxTBZ03A
    ML610405P-xxxTBZ03A
    ML610406P-xxxTBZ03A

    xxx: ROM code number (xxx is NNN for blank product)
    P: Wide range temperature version
    WA: Chip
    TBZ03A: TQFP

- Guaranteed operating range
  - Operating temperature: –40°C to +85°C
  - Operating voltage: V_{DD} = 1.25V to 3.6V

BLOCK DIAGRAM

ML610404/5/6 Block Diagram

Figure 1 show the block diagram of the ML610404/ML610405/ML610406.
"*" indicates the secondary function of each port.
"(*1)": 21seg×5com, 22seg×4com, 23seg×3com, and 24seg×2com selectable
"(*2)": 25seg×5com, 26seg×4com, 27seg×3com, and 28seg×2com selectable
"(*3)": 29seg×5com, 30seg×4com, 31seg×3com, and 32seg×2com selectable

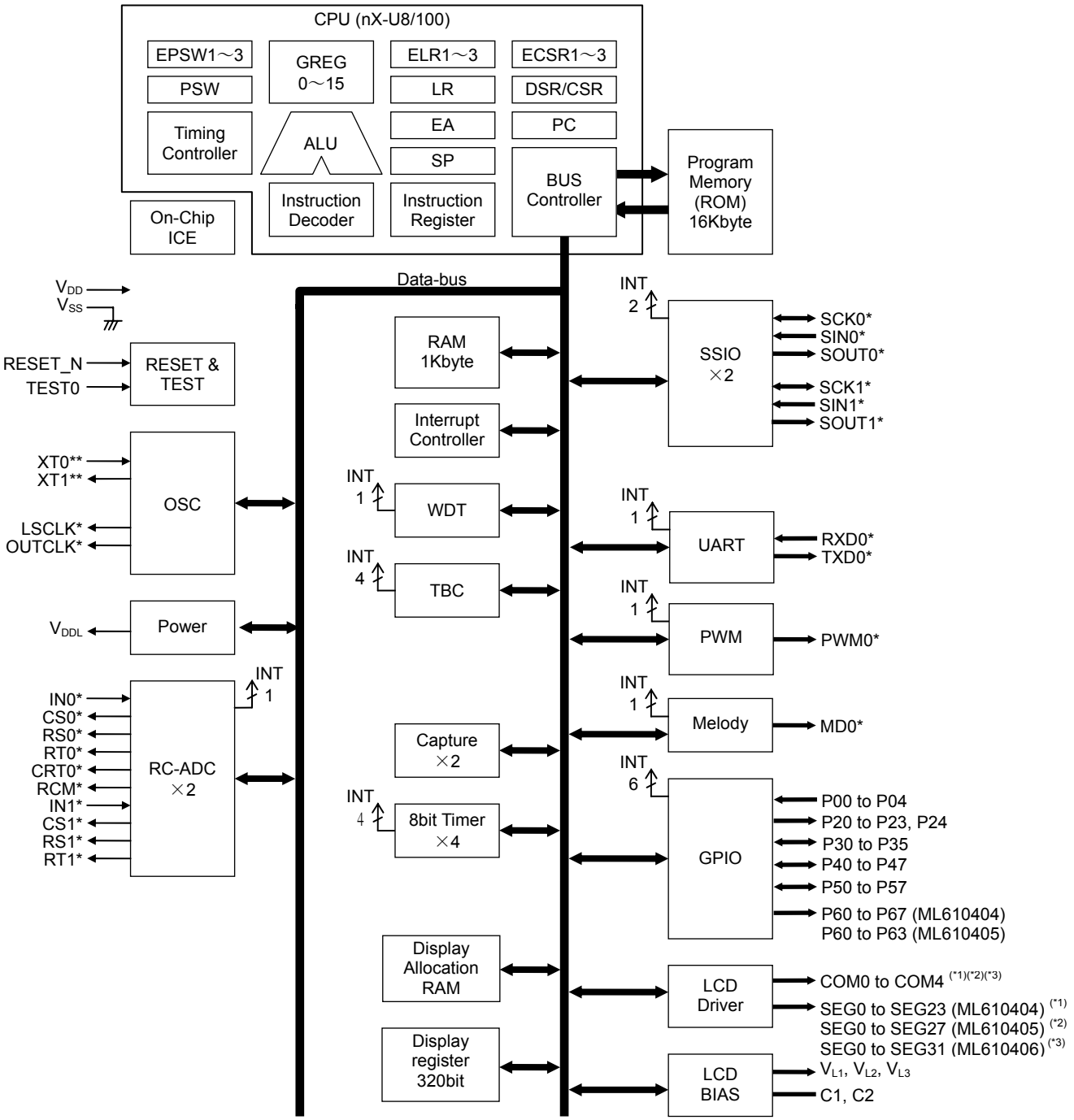
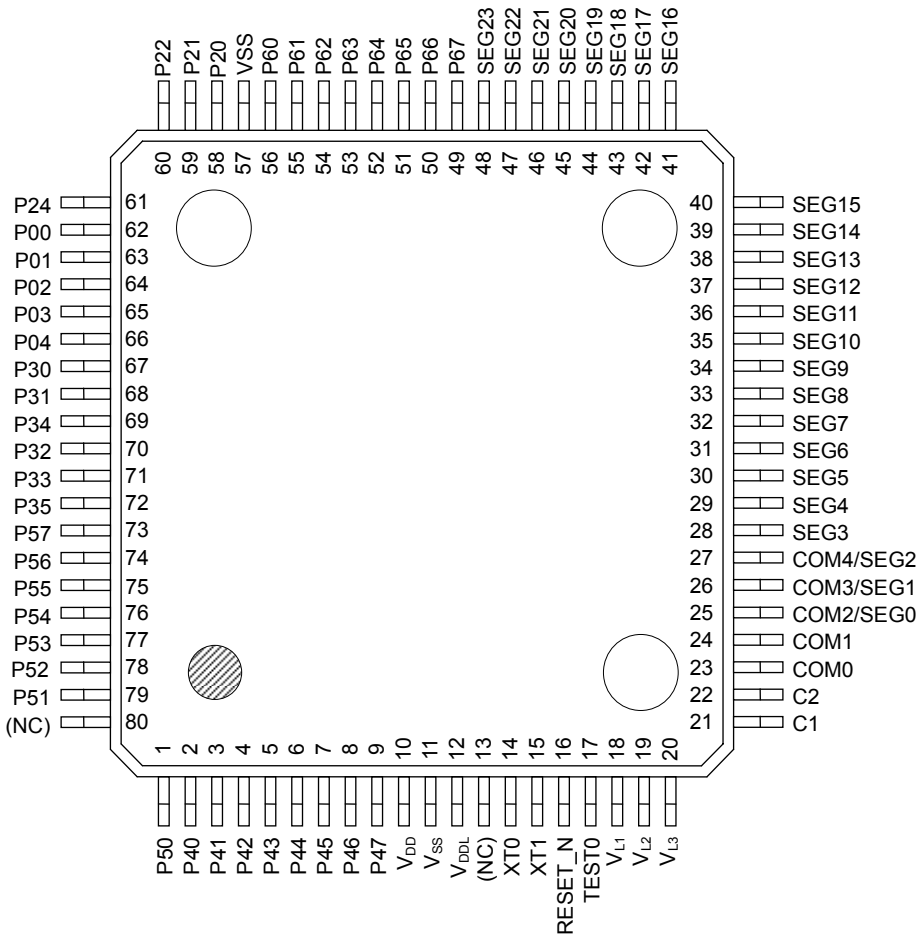


Figure 1 ML610404/ML610405/ML610406 Block Diagram

PIN CONFIGURATION

ML610404 TQFP80 Pin Layout

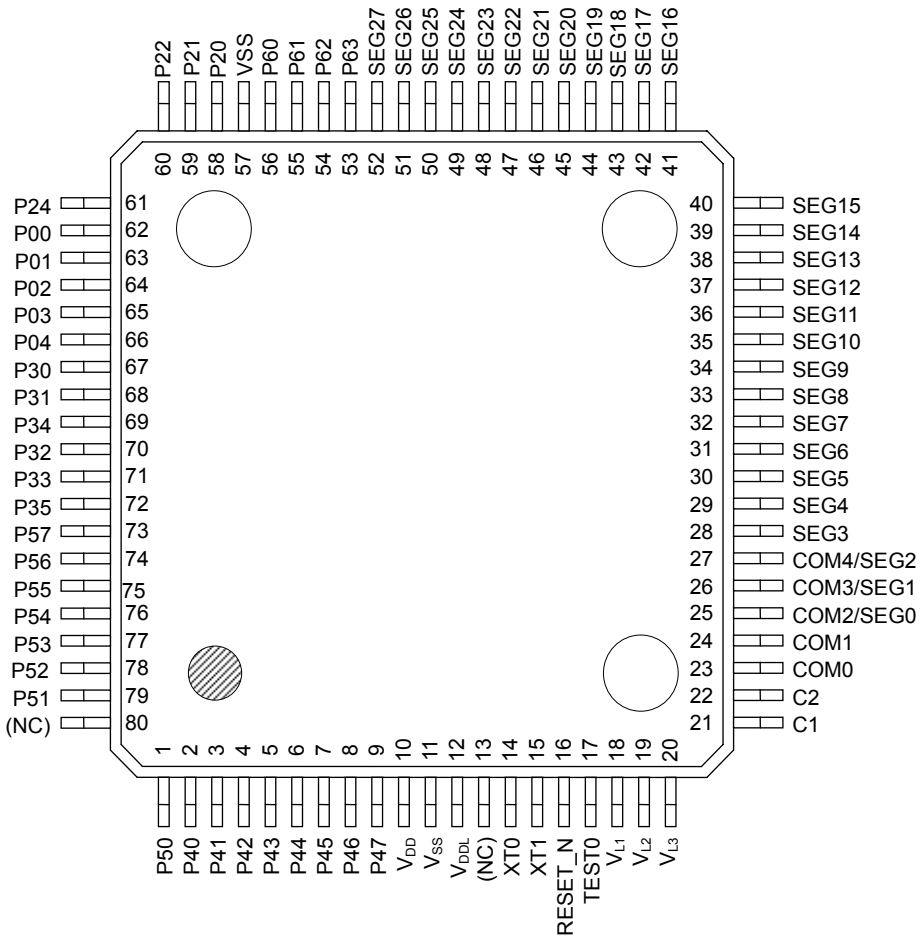


(NC): No Connection

Note:
The assignment of the P30 to P35 are not in order.

Figure 2 ML610404 TQFP80 Pin Configuration

ML610405 TQFP80 Pin Layout

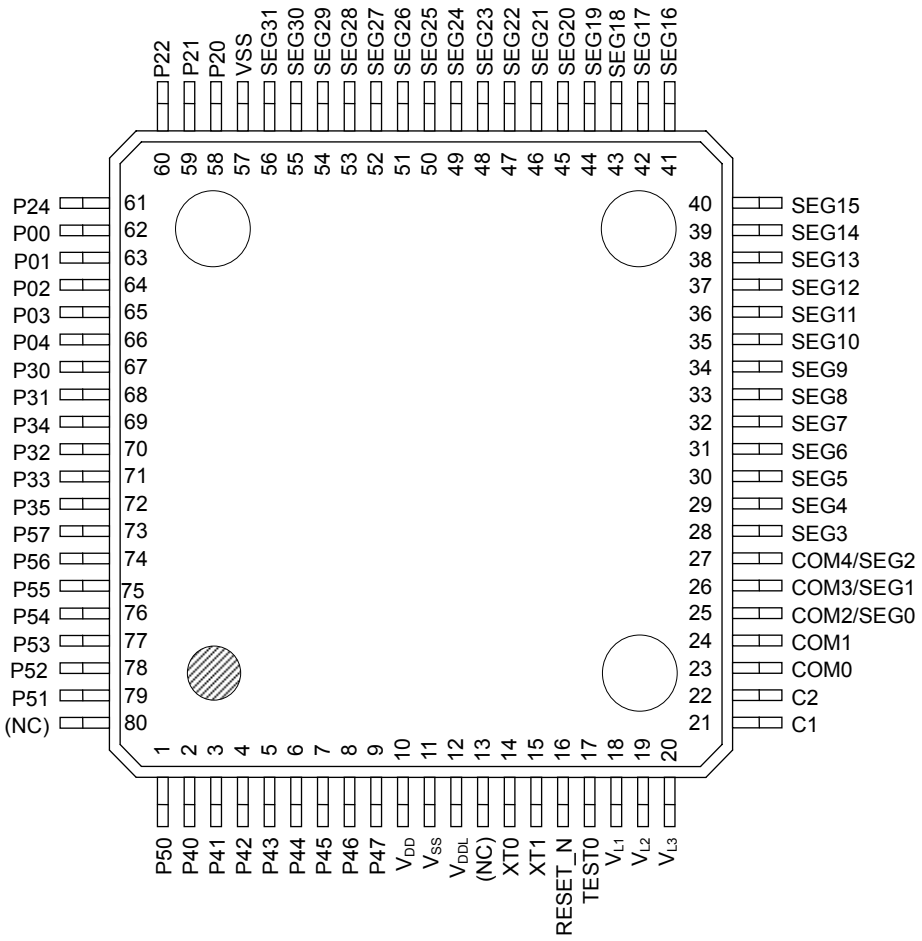


(NC): No Connection

Note:
The assignment of the P30 to P35 are not in order.

Figure 3 ML610405 TQFP80 Pin Configuration

ML610406 TQFP80 Pin Layout

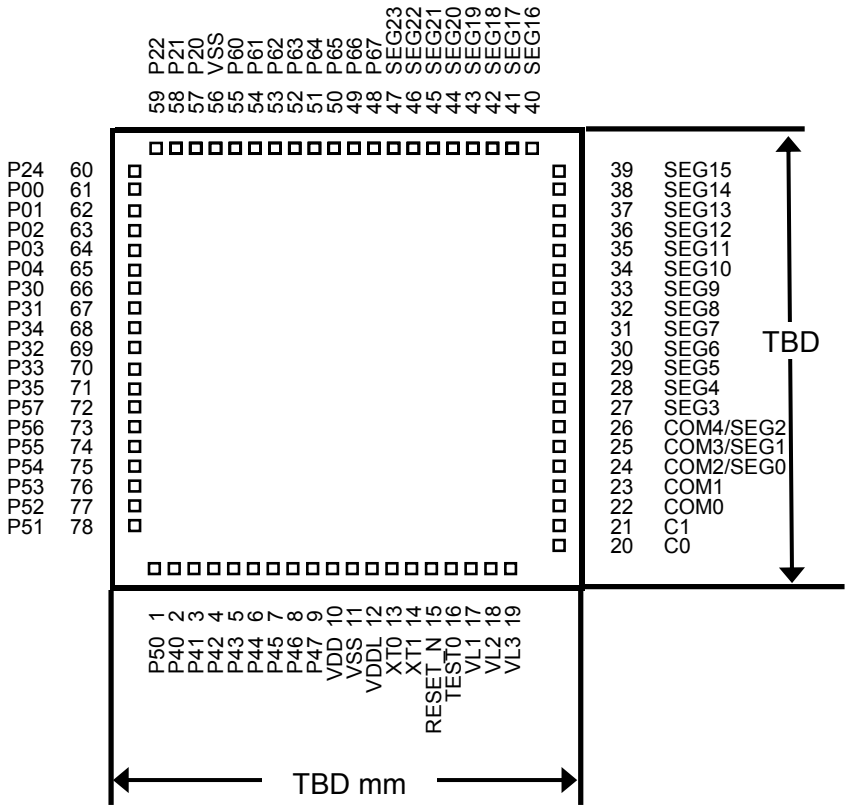


(NC): No Connection

Note:
The assignment of the P30 to P35 are not in order.

Figure 4 ML610406 TQFP80 Pin Configuration

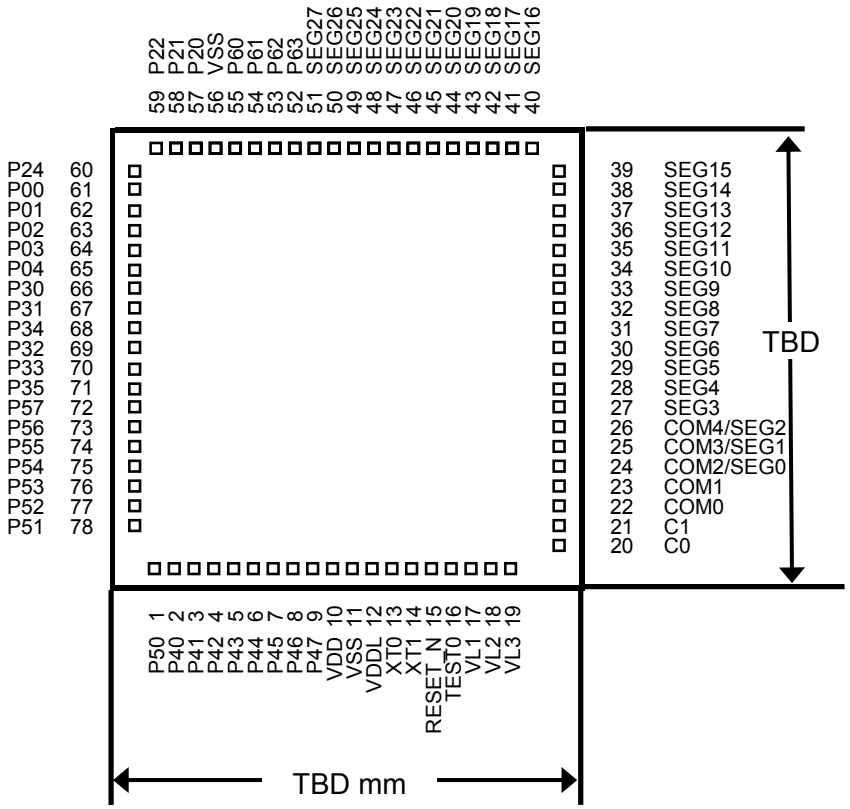
ML610404 Chip Pin Layout & Dimension



Chip size:	TBD mm x TBD mm
PAD count:	78 pins
Minimum PAD pitch:	80 μm
PAD aperture:	70 μm × 70 μm
Chip thickness:	350 μm
Voltage of the rear side of chip:	V_{SS} level

Figure 5 ML610404 Chip Layout & Dimension

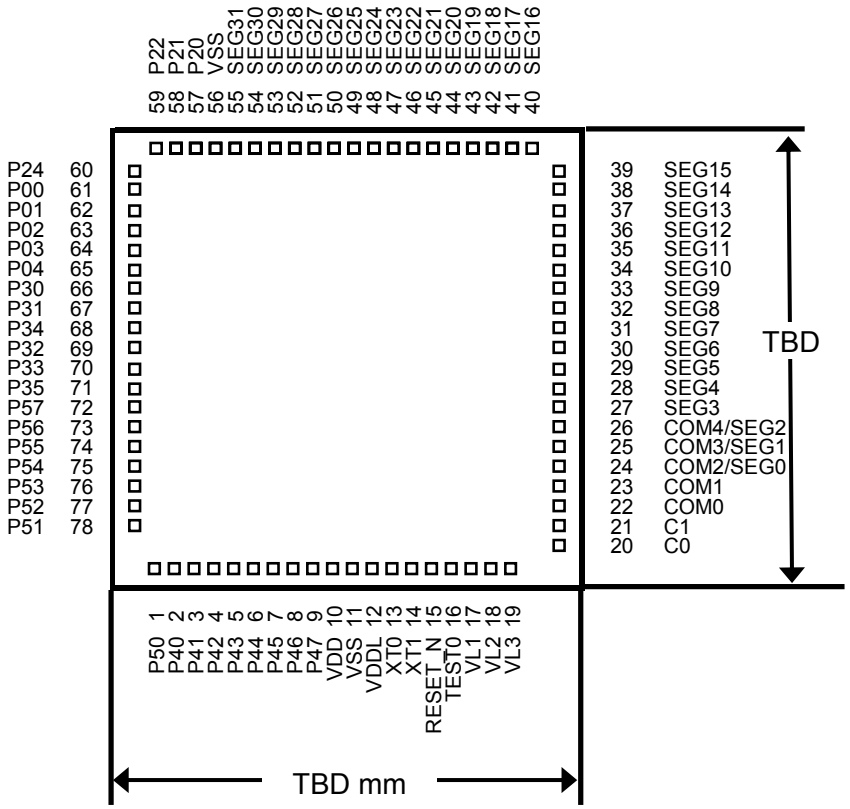
ML610405 Chip Pin Layout & Dimension



Chip size:	TBD mm x TBD mm
PAD count:	78 pins
Minimum PAD pitch:	80 μm
PAD aperture:	70 μm × 70 μm
Chip thickness:	350 μm
Voltage of the rear side of chip:	V_{SS} level

Figure 6 ML610405 Chip Layout & Dimension

ML610406 Chip Pin Layout & Dimension



Chip size:	TBD mm x TBD mm
PAD count:	78 pins
Minimum PAD pitch:	80 μm
PAD aperture:	70 μm × 70 μm
Chip thickness:	350 μm
Voltage of the rear side of chip:	V_{SS} level

Figure 7 ML610406 Chip Layout & Dimension

ML610404/ML610405/ML610406 Pad Coordinates (TBD)

Table 1 ML610404/ML610405/ML610406 Pad Coordinates

Chip Center: X=0,Y=0

PAD No.	Pad Name	ML610404/5/6	
		X (µm)	Y (µm)
1	P50		
2	P40		
3	P41		
4	P42		
5	P43		
6	P44		
7	P45		
8	P46		
9	P47		
10	VDD		
11	VSS		
12	VDDL		
13	XT0		
14	XT1		
15	RESET_N		
16	TEST0		
17	VL1		
18	VL2		
19	VL3		
20	C0		
21	C1		
22	COM0		
23	COM1		
24	COM2/SEG0		
25	COM3/SEG1		
26	COM4/SEG2		
27	SEG3		
28	SEG4		
29	SEG5		
30	SEG6		
31	SEG7		
32	SEG8		
33	SEG9		
34	SEG10		
35	SEG11		
36	SEG12		
37	SEG13		
38	SEG14		
39	SEG15		
40	SEG16		
41	SEG17		
42	SEG18		
43	SEG19		
44	SEG20		

PAD No.	Pad Name	ML610404/5/6	
		X (µm)	Y (µm)
45	SEG21		
46	SEG22		
47	SEG23		
48	P67 (*1)		
	SEG27 (*2)(*3)		
49	P66 (*1)		
	SEG27 (*2)(*3)		
50	P65 (*1)		
	SEG27 (*2)(*3)		
51	P64 (*1)		
	SEG27 (*2)(*3)		
52	P63 (*1)(*2)		
	SEG28 (*3)		
53	P62 (*1)(*2)		
	SEG29 (*3)		
54	P61 (*1)(*2)		
	SEG30 (*3)		
55	P60 (*1)(*2)		
	SEG31 (*3)		
56	VSS		
57	P20		
58	P21		
59	P22		
60	P24		
61	P00		
62	P01		
63	P02		
64	P03		
65	P04		
66	P30		
67	P31		
68	P34		
69	P32		
70	P33		
71	P35		
72	P57		
73	P56		
74	P55		
75	P54		
76	P53		
77	P52		
78	P51		

(*1) ML610404 pad name, (*2) ML610405 pad name, (*3) ML610406 pad name

PIN LIST

PIN No.	PAD No.	Primary function			Secondary function/ Tertiary function			
		Pin name	I/O	Function	Secondary/ Tertiary	Pin name	I/O	Function
11,57	11,56	V_{SS}	—	Negative power supply pin	—	—	—	—
10	10	V_{DD}	—	Positive power supply pin	—	—	—	—
12	12	V_{DDL}	—	Power supply pin for internal logic (internally generated)	—	—	—	—
18	17	V_{L1}	—	Power supply pin for LCD bias (internally generated or connected positive power supply pin) (*1)	—	—	—	—
19	18	V_{L2}	—	Power supply pin for LCD bias (internally generated or connected positive power supply pin) (*1)	—	—	—	—
20	19	V_{L3}	—	Power supply pin for LCD bias (internally generated or connected positive power supply pin) (*1)	—	—	—	—
21	20	C1	—	Capacitor connection pin for LCD bias generation	—	—	—	—
22	21	C2	—	Capacitor connection pin for LCD bias generation	—	—	—	—
17	16	TEST0	I/O	Input/output pin for testing	—	—	—	—
16	15	RESET_N	I	Reset input pin	—	—	—	—
14	13	XT0	I	Low-speed clock oscillation pin	—	—	—	—
15	14	XT1	O	Low-speed clock oscillation pin	—	—	—	—
62	61	P00/EXI0/ CAP0	I	Input port, External interrupt 0, Capture 0 input	—	—	—	—
63	62	P01/EXI1/ CAP1	I	Input port, External interrupt 1, Capture 1 input	—	—	—	—
64	63	P02/EXI2/ RXD0	I	Input port, External interrupt 2, UART0 receive	—	—	—	—
65	64	P03/EXI3	I	Input port, External interrupt 3	—	—	—	—
66	65	P04/ T0P0CK/ EXI4	I	input port, timer0/PWM0 external clock input	—	—	—	—
58	57	P20/LED0	O	Output port	Secondary	LSCLK	O	Low-speed clock output
59	58	P21LED1	O	Output port	Secondary	OUTCLK	O	High-speed clock output
60	59	P22/LED2	O	Output port	Secondary	MD0	O	Melody output
61	60	P24/LED4	O	Output port	Secondary	PWM0	O	PWM output
67	66	P30	I/O	Input/output port	Secondary	IN0	I	RC type ADC0 oscillation input pin
68	67	P31	I/O	Input/output port	Secondary	CS0	O	RC type ADC0 reference capacitor connection pin
69	68	P34	I/O	Input/output port	Secondary	RCT0	O	RC type ADC0 resistor/capacitor sensor connection pin
70	69	P32	I/O	Input/output port	Secondary	RS0	O	RC type ADC0 reference resistor connection pin
71	70	P33	I/O	Input/output port	Secondary	RT0	O	RC type ADC0 resistor sensor connection pin
72	71	P35	I/O	Input/output port	Secondary	RCM	O	RC type ADC oscillation monitor
2	2	P40	I/O	Input/output port	Secondary	—	—	—
					Tertiary	SIN0	I	SSIO data input
3	3	P41	I/O	Input/output port	Secondary	—	—	—
					Tertiary	SCK0	I/O	SSIO synchronous clock
4	4	P42	I/O	Input/output port	Secondary	RXD0	I	UART data input
					Tertiary	SOUT0	I	SSIO data output

PIN No.	PAD No.	Primary function			Secondary function/ Tertiary function			
		Pin name	I/O	Function	Secondary/ Tertiary	Pin name	I/O	Function
5	5	P43	I/O	Input/output port	Secondary	TXD0	O	UART data output
					Tertiary	PWM0	O	PWM output
6	6	P44/ T02P0CK	I/O	Input/output port, Timer 0//PWM0 external clock input	Secondary	IN1	I	RC type ADC1 oscillation input pin
					Tertiary	SIN0	I	SSIO0 data input
7	7	P45/ T13CK	I/O	Input/output port, Timer 1 external clock input	Secondary	CS1	O	RC type ADC1 reference capacitor connection pin
					Tertiary	SCK0	I/O	SSIO0 synchronous clock
8	8	P46	I/O	Input/output port	Secondary	RS1	O	RC type ADC1 reference resistor connection pin
					Tertiary	SOUT0	O	SSIO0 data output
9	9	P47	I/O	Input/output port	Secondary	RT1	O	RC type ADC1 resistor sensor connection pin
1	1	P50/EXI8	I/O	Input/output port, External interrupt 8	Secondary	SIN1	I	SSIO1 data input
79	78	P51/EXI8	I/O	Input/output port, External interrupt 8	Secondary	SCK1	I/O	SSIO1 synchronous clock
78	77	P52/EXI8	I/O	Input/output port, External interrupt 8	Secondary	SOUT1	I	SSIO1 data output
77	76	P53/EXI8	I/O	Input/output port, External interrupt 8	Secondary	MD0	O	Melody output
76	75	P54/EXI8	I/O	Input/output port, External interrupt 8	—	—	—	—
75	74	P55/EXI8	I/O	Input/output port, External interrupt 8	—	—	—	—
74	73	P56/EXI8	I/O	Input/output port, External interrupt 8	—	—	—	—
73	72	P57/EXI8	I/O	Input/output port, External interrupt 8	—	—	—	—
23	22	COM0	O	LCD common pin	—	—	—	—
24	23	COM1	O	LCD common pin	—	—	—	—
25	24	COM2/ SEG0	O	LCD common/segment pin (*5)	—	—	—	—
26	25	COM3/ SEG1	O	LCD common/segment pin (*5)	—	—	—	—
27	26	COM4/ SEG2	O	LCD segment/segment pin (*5)	—	—	—	—
28	27	SEG3	O	LCD segment pin	—	—	—	—
29	28	SEG4	O	LCD segment pin	—	—	—	—
30	29	SEG5	O	LCD segment pin	—	—	—	—
31	30	SEG6	O	LCD segment pin	—	—	—	—
32	31	SEG7	O	LCD segment pin	—	—	—	—
33	32	SEG8	O	LCD segment pin	—	—	—	—
34	33	SEG9	O	LCD segment pin	—	—	—	—
35	34	SEG10	O	LCD segment pin	—	—	—	—
36	35	SEG11	O	LCD segment pin	—	—	—	—
37	36	SEG12	O	LCD segment pin	—	—	—	—
38	37	SEG13	O	LCD segment pin	—	—	—	—
39	38	SEG14	O	LCD segment pin	—	—	—	—
40	39	SEG15	O	LCD segment pin	—	—	—	—
41	40	SEG16	O	LCD segment pin	—	—	—	—
42	41	SEG17	O	LCD segment pin	—	—	—	—
43	42	SEG18	O	LCD segment pin	—	—	—	—
44	43	SEG19	O	LCD segment pin	—	—	—	—
45	44	SEG20	O	LCD segment pin	—	—	—	—
46	45	SEG21	O	LCD segment pin	—	—	—	—
47	46	SEG22	O	LCD segment pin	—	—	—	—
48	47	SEG23	O	LCD segment pin	—	—	—	—
49	48	P67 (*2)	O	Output port	—	—	—	—
		SEG24(*3)(*4)		LCD segment pin	—	—	—	—

PIN No.	PAD No.	Primary function			Secondary function/ Tertiary function			
		Pin name	I/O	Function	Secondary/ Tertiary	Pin name	I/O	Function
50	49	P66 (*2)	O	Output port	—	—	—	—
		SEG25(*3)(*4)		LCD segment pin	—	—	—	—
51	50	P65 (*2)	O	Output port	—	—	—	—
		SEG26(*3)(*4)		LCD segment pin	—	—	—	—
52	51	P64 (*2)	O	Output port	—	—	—	—
		SEG27(*3)(*4)		LCD segment pin	—	—	—	—
53	52	P63 (*2) (*3)	O	Output port	—	—	—	—
		SEG28 (*4)		LCD segment pin	—	—	—	—
54	53	P62 (*2) (*3)	O	Output port	—	—	—	—
		SEG29 (*4)		LCD segment pin	—	—	—	—
55	54	P61 (*2) (*3)	O	Output port	—	—	—	—
		SEG30 (*4)		LCD segment pin	—	—	—	—
56	55	P60 (*2) (*3)	O	Output port	—	—	—	—
		SEG31 (*4)		LCD segment pin	—	—	—	—

(*1) The details of the power supply are shown in the user's manual.
(*2) Pins on ML610404
(*3) Pins on ML610405
(*4) Pins on ML610406
(*5) Either LCD common or segment can be selected by the software.

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, system reset mode is set and the internal section is initialized. When this pin is set to a “H” level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
XT0	I	Crystal connection pin for low-speed clock.	—	—
XT1	O	A 32.768 kHz crystal oscillator (see measuring circuit 1) is connected to this pin. Capacitors CDL and CGL are connected across this pin and V_{SS} .	—	—
LSCLK	O	Low-speed clock output pin. This pin is used as the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the secondary function of the P21 pin.	Secondary	—
General-purpose input port				
P00-P04	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose output port				
P20-P22,P24	O	General-purpose output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose input/output port				
P30-P35	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P40-P47	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P50-P57	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P60-P63	O	General-purpose input/output port. These pins are for the ML610404/ML610405, but are not provided in the ML610406.	Primary	Positive
P64-P67	O	General-purpose input/output port. These pins are for the ML610404, but are not provided in the ML610405/ML610406.	Primary	Positive

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
UART				
TXD0	O	UART data output pin. This pin is used as the secondary function of the P43 pin.	Secondary	Positive
RXD0	I	UART data input pin. This pin is used as the secondary function of the P42 or the primary function of the P02 pin.	Primary/Secondary	Positive
Synchronous serial (SSIO)				
SCK0	I/O	Synchronous serial clock input/output pin. This pin is used as the tertiary function of the P41 or P45 pin.	Tertiary	—
SIN0	I	Synchronous serial data input pin. This pin is used as the tertiary function of the P40 or P44 pin.	Tertiary	Positive
SOUT0	O	Synchronous serial data output pin. This pin is used as the tertiary function of the P42 or P46 pin.	Tertiary	Positive
SCK1	I/O	Synchronous serial clock input/output pin. This pin is used as the secondary function of the P51 pin.	Secondary	—
SIN1	I	Synchronous serial data input pin. This pin is used as the secondary function of the P50.	Secondary	Positive
SOUT1	O	Synchronous serial data output pin. This pin is used as the secondary function of the P52 pin.	Secondary	Positive
PWM				
PWM0	O	PWM0 output pin. This pin is used as the tertiary function of the P43 or P34 pin.	Tertiary	Positive
T02P0CK	O	PWM0 external clock input pin. This pin is used as the primary function of the P44 pin.	Primary	—
External interrupt				
EXI0-4	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P00-P04 pins.	Primary	Positive/ negative
EXI8	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P50-P57 pins.	Primary	Positive/ negative
Capture				
CAP0	I	Capture trigger input pins. The value of the time base counter is captured in the register synchronously with the interrupt edge selected by software. These pins are used as the primary functions of the P00 pin(CAP0) and P01 pin(CAP1).	Primary	Positive/ negative
CAP1	I		Primary	Positive/ negative
Timer				
T0P0CK	I	External clock input pin used for Timer 0. The clock for this timer is selected by software. This pin is used as the primary function of the P44 pin.	Primary	—
T1CK	I	External clock input pin used both Timer 1. The clock for this timer is selected by software. This pin is used as the primary function of the P45 pin.	Primary	—
Melody				
MD0	O	Melody/Buzzer signal output pin. This pin is used as the secondary function of the P22 pin and P53 pin.	Secondary	Positive/ negative
LED drive				
LED0-2,4	O	Nch open drain output pins to drive LED.	Primary	Positive/ negative

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
RC oscillation type A/D converter				
IN0	I	Channel 0 oscillation input pin. This pin is used as the secondary function of the P30 pin.	Secondary	—
CS0	O	Channel 0 reference capacitor connection pin. This pin is used as the secondary function of the P31 pin.	Secondary	—
RCT0	O	Resistor/capacitor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P33 pin.	Secondary	—
RS0	O	This pin is used as the secondary function of the P32 pin which is the reference resistor connection pin of Channel 0.	Secondary	—
RT0	O	Resistor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P34 pin.	Secondary	—
RCM	O	RC oscillation monitor pin. This pin is used as the secondary function of the P35 pin.	Secondary	—
IN1	I	Oscillation input pin of Channel 1. This pin is used as the secondary function of the P44 pin.	Secondary	—
CS1	O	Reference capacitor connection pin of Channel 1. This pin is used as the secondary function of the P45 pin.	Secondary	—
RS1	O	Reference resistor connection pin of Channel 1. This pin is used as the secondary function of the P46 pin.	Secondary	—
RT1	O	Resistor sensor connection pin for measurement of Channel 1. This pin is used as the secondary function of the P47 pin.	Secondary	—
LCD drive signal				
COM0-4	O	Common output pins.	—	—
SEG0-23	O	Segment output pins.	—	—
SEG24-27	O	Segment output pin. These pins are for the ML610405/ML610406, but are not provided in the ML610404.	—	—
SEG28-31	O	Segment output pin. These pins are for the ML610406, but are not provided in the ML610404/ML610405.	—	—
LCD driver power supply				
V_{L1}	—	Power supply pins for LCD bias (internally generated or positive power supply pin connected). Capacitors Ca, Cb, and Cc (see measuring circuit 1) are connected between V_{SS} and V_{L1}, V_{L2}, and V_{L3}, respectively.	—	—
V_{L2}	—		—	—
V_{L3}	—		—	—
C1	—	Power supply pins for LCD bias (internally generated). Capacitors C12 is connected between C1 and C2.	—	—
C2	—		—	—
For testing				
TEST	I/O	Input/output pin for testing. A pull-down resistor is internally connected.	—	—
Power supply				
V_{SS}	—	Negative power supply pin.	—	—
V_{DD}	—	Positive power supply pin for I/O, internal regulator, battery low detector, and power-on reset.	—	—
V_{DDL}	—	Positive power supply pin (internally generated) for internal logic. Capacitor CL (see measuring circuit 1) is connected between this pin and V_{SS}.	—	—

TERMINATION OF UNUSED PINS

Table 3 shows methods of terminating the unused pins.

Table 3 Termination of Unused Pins

Pin	Recommended pin termination
V_{PP}	Open
V_{L1}, V_{L2}, V_{L3}	Open
C1, C2	Open
RESET_N	Open
TEST0	Open
P00 to P04	V_{DD} or V_{SS}
P20 to P22, P24	Open
P30 to P35	Open
P40 to P47	Open
P50 to P57	Open
P60 to P67	Open
COM0 to 4	Open
SEG0 to 31	Open

Note:
It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta = 25°C	−0.3 to +4.6	V
Power supply voltage 2	V_{PP}	Ta = 25°C	−0.3 to +9.5	V
Power supply voltage 3	V_{DDL}	Ta = 25°C	−0.3 to +3.6	V
Power supply voltage 4	V_{L1}	Ta = 25°C	−0.3 to +2.0	V
Power supply voltage 5	V_{L2}	Ta = 25°C	−0.3 to +4.0	V
Power supply voltage 6	V_{L3}	Ta = 25°C	−0.3 to +6.0	V
Input voltage	V_{IN}	Ta = 25°C	−0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta = 25°C	−0.3 to V_{DD}+0.3	V
Output current 1	I_{OUT1}	Port3–6, Ta = 25°C	−12 to +11	mA
Output current 2	I_{OUT2}	Port2, Ta = 25°C	−12 to +20	mA
Power dissipation	PD	Ta = 25°C	0.9	W
Storage temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	—	−40 to +85	°C
Operating voltage	V_{DD}	f_{OP} = 30k to 625kHz	1.25 to 3.6	V
		f_{OP} = 30k to 2.5MHz	1.8 to 3.6	
Operating frequency (CPU)	f_{OP}	V_{DD} = 1.25 to 3.6V	30k to 625k	Hz
		V_{DD} = 1.8 to 3.6V	30k to 2.5M	
Low-speed crystal oscillation frequency	f_{XTL}	—	32.768k	Hz
Low-speed crystal oscillation external capacitor	C_{DL}	—	5 to 25 (TBD)	pF
	C_{GL}	—	5 to 25 (TBD)	
Capacitor externally connected to V_{DDL} pin	C_L	—	0.47±30%	µF
Capacitors externally connected to $V_{L1, 2, 3}$ pins	$C_{a, b, c}$	—	0.1±30%	µF
Capacitors externally connected across C1 and C2 pins	C_{12}	—	0.47±30%	µF

OPERATING CONDITIONS OF FLASH ROM

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	At write/erase	0 to +40	°C
Operating voltage	V_{DD}	At write/erase*1	2.75 to 3.6	V
	V_{DDL}	At write/erase*1	2.5 to 2.75	
	V_{PP}	At write/erase*1	7.7 to 8.3	
erase/program cycles	C_{EP}	—	80	cycles
Data retention	Y_{DR}	—	10	years

*1: Those voltages must be supplied to V_{DDL} pin and V_{PP} pin when programming and eraseing Flash ROM. V_{PP} pin has an internal pulldown resister.

DC CHARACTERISTICS (1/5)

(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = −40 to +85°C, unless otherwise specified)

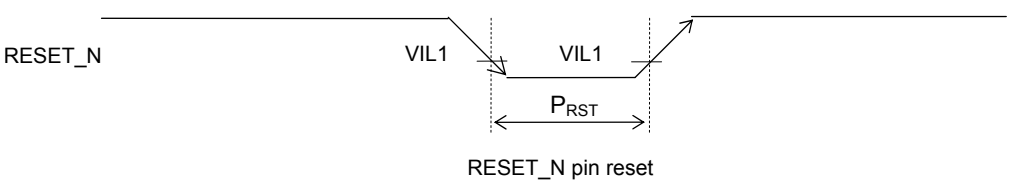
Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
500kHz/2MHz RC oscillation frequency	f_{RC}	V_{DD} = 1.25 to 3.6V	Ta = 25°C	Typ. −10%	500	Typ. +10%	kHz	1
			*3	Typ. −25%	500	Typ. +25%		
		V_{DD} = 1.80 to 3.6V	Ta = 25°C	Typ. −10%	2.0	Typ. +10%	MHz	
			*3	Typ. −25%	2.0	Typ. +25%		
Low-speed crystal oscillation start time*2	T_{XTL}	—		—	0.6	2	s	
500kHz/2MHz RC oscillation start time	T_{RC}	—		—	—	3	μs	
Low-speed oscillation stop detect time*1	T_{STOP}	—		12	16.4	41	ms	
Reset pulse width	P_{RST}	—		200	—	—	μs	
Reset noise elimination pulse width	P_{NRST}	—		—	—	0.3		
Power-on reset activation power rise time	T_{POR}	—		—	—	10	ms	

*1: When low-speed crystal oscillation stops for a duration more than the low-speed oscillation stop detect time, the system is reset to shift to system reset mode.

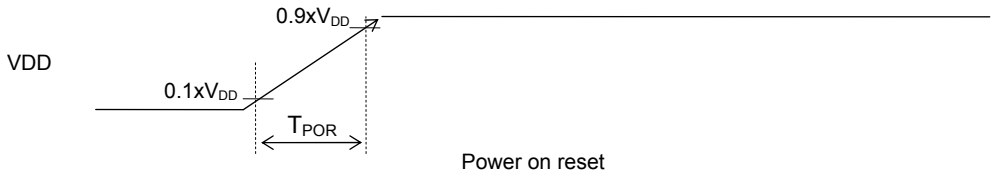
*2 : 32.768KHz Crystal resonator DT-26 (Load Capacitance 6pF) (made by KDS: DAISHINKU CORP.) is used (C_{GL}=C_{DL}= TBD pF)

*3 : Recommended operating temperature (Ta = −40 to +85°C)

RESET



RESET_N pin reset



Power on reset

DC CHARACTERISTICS (2/5)

(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
V_{DDL} voltage	V_{DDL}	f_{OP} = 30k to 625kHz	1.1	1.2	1.3	V	1
		f_{OP} = 30k to 2.5MHz	1.35	1.5	1.65		
V_{DDL} temperature deviation *1	ΔV_{DDL}	V_{DD} = 3.0V	—	-1	—	mV/°C	
V_{DDL} voltage dependency *1	ΔV_{DDL}	—	—	5	20	mV/V	

*1:V_{DDL} can not exceed V_{DD} level. The maximum V_{DDL} becomes V_{DD} level when the V_{DDL} calculated by the temperature deviation and voltage dependency is going to exceed the V_{DD} level.

DC CHARACTERISTICS (3/5)

(V_{DD} = 3.0V, V_{SS} = 0V, Ta = –40 to +85°C)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed RC500kHz/2MHz oscillation: stopped.	Ta= 25°C	—	0.3	0.8	μA	1
			*5	—	—	3		
Supply current 2	IDD2	CPU: In HALT state (LTBC and WDT are Operating.).*3*4 High-speed 500kHz/2MHz oscillation: Stopped. LCD and BIAS circuits: Operating. *6	Ta= 25°C	—	0.9	1.8	μA	
			*5	—	—	4		
Supply current 3	IDD3	CPU: In 32.768kHz operating state.*1*3 High-speed 500kHz/2MHz oscillation: Stopped. LCD and BIAS circuits: Operating. *2	Ta= 25°C	—	6	9	μA	
			*5	—	—	15		
Supply current 4-1	IDD4-1	CPU: In RC 500kHz operating state. LCD and BIAS circuits: Operating. *2	Ta= 25°C	—	80	100	μA	1
			*5	—	—	120		
Supply current 4-2	IDD4-2	CPU: In RC 2MHz operating state. LCD and BIAS circuits: Operating. *2	Ta= 25°C	—	0.4	0.5	mA	
			*5	—	—	0.6		

*1: When the CPU operating rate is 100% (No HALT state).
*2: All SEGs: off waveform, No LCD panel load, 1/3 bias, 1/3 duty, Frame frequency: Approx. 64 Hz, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)
*3 : Use 32.768KHz Crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used (C_{GL}=C_{DL}=TBD pF).
*4 : Significant bits of BLKCON0 to BLKCON4 registers are all “1” except DLCD bit on BLKCON4.
*5 : Recommended operating temperature (Ta = –40 to +85°C)
*6 : LCD stop mode, 1/3 bias, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)

DC CHARACTERISTICS (4/5)

(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Output voltage 1 (P20–P22,P24(N-channel open drain output is not selected)) (P30–P35) (P40–P47) (P50–P57) (P60-P63) *1 *2 (P64-P67) *1	VOH1	IOH1 = –0.5mA, V_{DD} = 1.8 to 3.6V	V_{DD} –0.5	—	—	V	2
		IOH1 = -0.1mA, V_{DD} = 1.25 to 3.6V	V_{DD} –0.3	—	—		
	VOL1	IOL1 = +0.5mA, V_{DD} = 1.8 to 3.6V	—	—	0.5		
		IOL1 = +0.1mA, V_{DD} = 1.25 to 3.6V	—	—	0.3		
Output voltage 2 (P20–P22,P24 (N-channel open drain output is not selected))	VOL2	IOL2 = +5mA, V_{DD} = 1.8 to 3.6V	—	—	0.5		
Output voltage 3 (COM0–4) (SEG0–23)*1 (SEG0–27)*2 (SEG0–31)*3	VOH3	IOH3 = –0.05mA, VL1=1.2V	V_{L3} –0.2	—	—		
	VOML3	IOML3 = +0.05mA, VL1=1.2V	—	—	V_{L2} +0.2		
	VOML3S	IOML3S = –0.05mA, VL1=1.2V	V_{L2} –0.2	—	—		
	VOLM3	IOLM3 = +0.05mA, VL1=1.2V	—	—	V_{L1} +0.2		
	VOLM3S	IOLM3S = –0.05mA, VL1=1.2V	V_{L1} –0.2	—	—		
	VOL3	IOL3 = +0.05mA, VL1=1.2V	—	—	0.2		
Output leakage (P20–P22, P24) (P30–P35) (P40–P47) (P50–P57) (P60-P63) *1 *2 (P64-P67) *1	IOOH	VOH = V_{DD} (in high-impedance state)	—	—	1	μA	3
	IOOL	VOL = V_{SS} (in high-impedance state)	–1	—	—		
Input current 1 (RESET_N)	IIH1	VIH1 = V_{DD}	—	—	1	μA	4
	IIL1	VIL1 = V_{SS}	-600	-300	-2		
Input current 2 (TEST0)	IIH2	VIH1 = V_{DD}	2	300	600		
	IIL2	VIL1 = V_{ss}	-1	—	—		
Input current 2 (P00-P04) (P30-P35) (P40-P47) (P50-P57)	IIH3	VIH3 = V_{DD}, V_{DD} = 1.8 to 3.6V (when pulled-down)	2	30	200		
		VIH3 = V_{DD}, V_{DD} = 1.25 to 3.6V (when pulled-down)	0.01	30	200		
	IIL3	VIL3 = V_{ss}, V_{DD} = 1.8 to 3.6V (when pulled-up)	-200	-30	-2		
		VIL3 = V_{ss}, V_{DD} = 1.25 to 3.6V (when pulled-up)	-200	-30	-0.01		
	IIH3Z	VIH3 = V_{DD} (in high-impedance state)	—	—	1		
	IIL3Z	VIL3 = V_{SS} (in high-impedance state)	–1	—	—		

*1: pins on ML610404
*2: pins on ML610405
*3: pins on ML610406

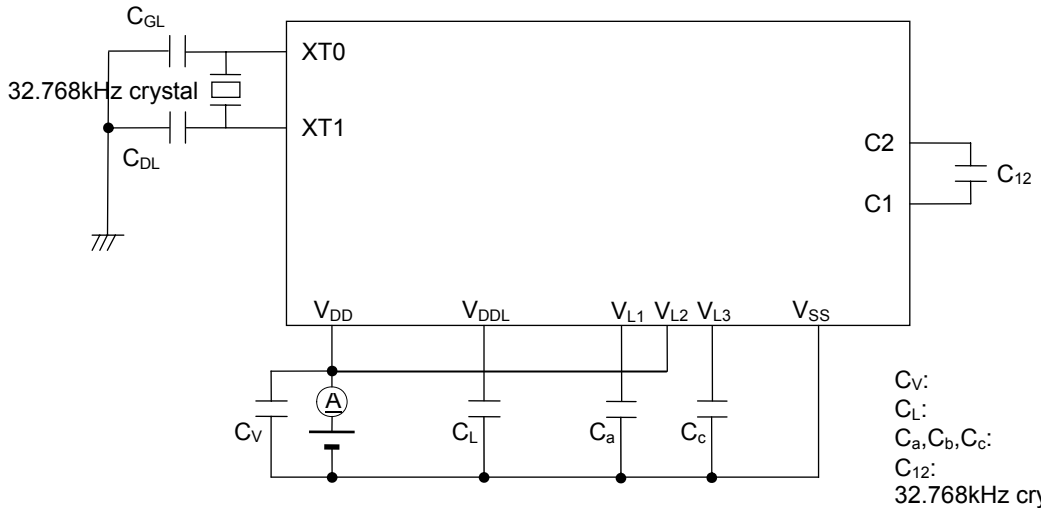
DC CHARACTERISTICS (5/5))

(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N) (TEST0) (P00–P04) (P30–P35) (P40–P47) (P50–P57)	VIH1	—	0.7 ×V_{DD}	—	V_{DD}	V	5
	VIL1	V_{DD} = 1.8 to 3.6V	0	—	0.3 ×V_{DD}		
		V_{DD} = 1.25 to 3.6V	0	—	0.2 ×V_{DD}		
Input pin capacitance (P00–P04) (P30–P35) (P40–P47) (P50–P57)	CIN	f = 10kHz V_{rms} = 50mV Ta = 25°C	—	—	5	pF	—

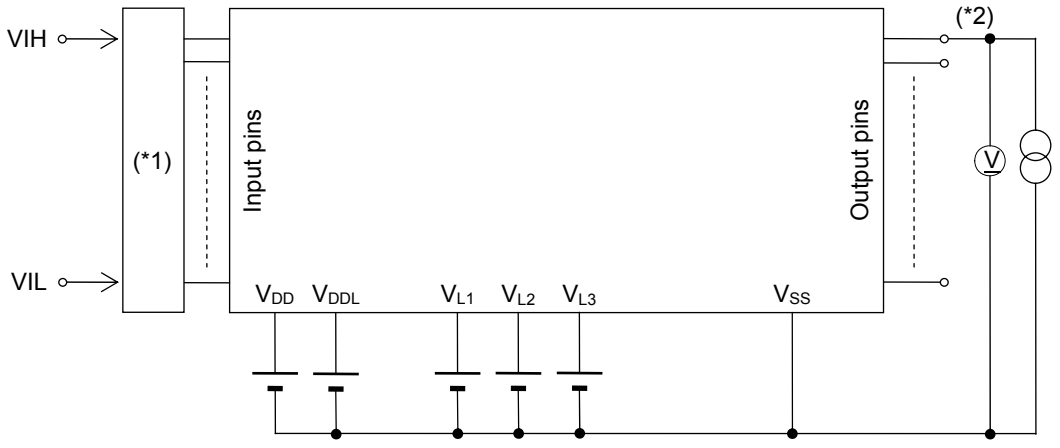
MEASURING CIRCUITS

MEASURING CIRCUIT 1



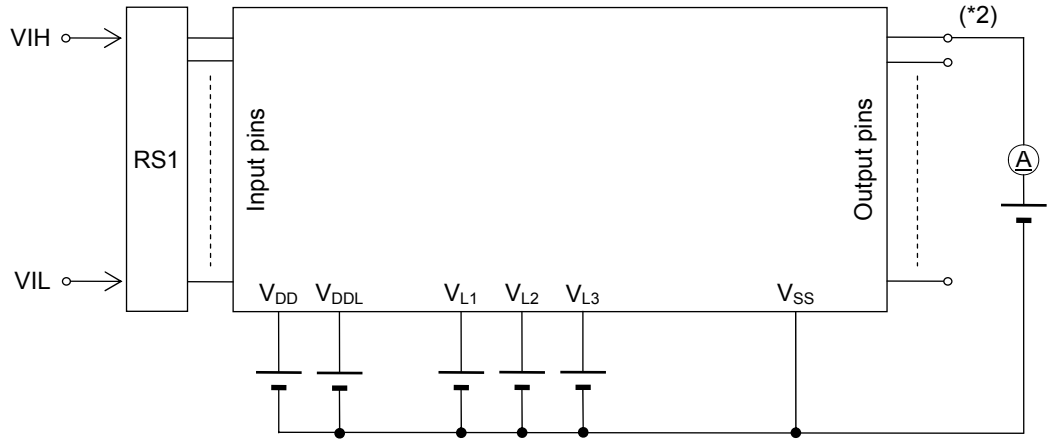
C_V: 1μF
C_L: 0.47μF
C_a,C_b,C_c: 0.1μF
C_{12}: 0.47μF
32.768kHz crystal resonator:
DT-26(Load capacitance 6pF)
(Made by KDS: DAISHINKU COP.)
C_{GL}, C_{DL}: 6pF(TBD)

MEASURING CIRCUIT 2



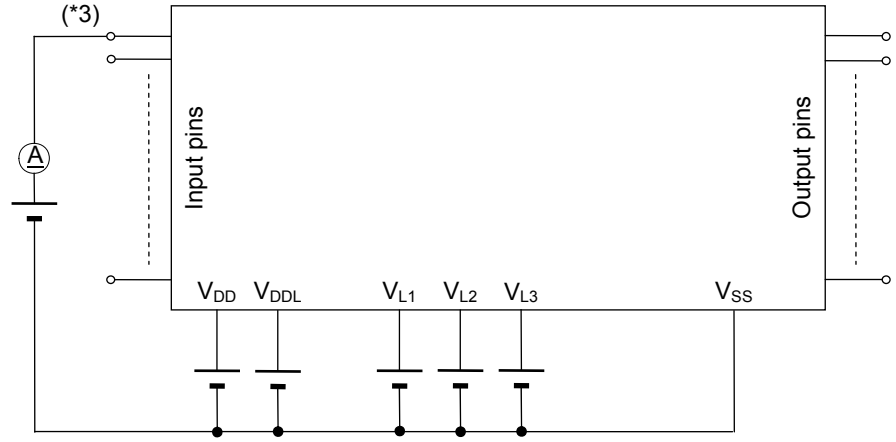
(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

MEASURING CIRCUIT 3



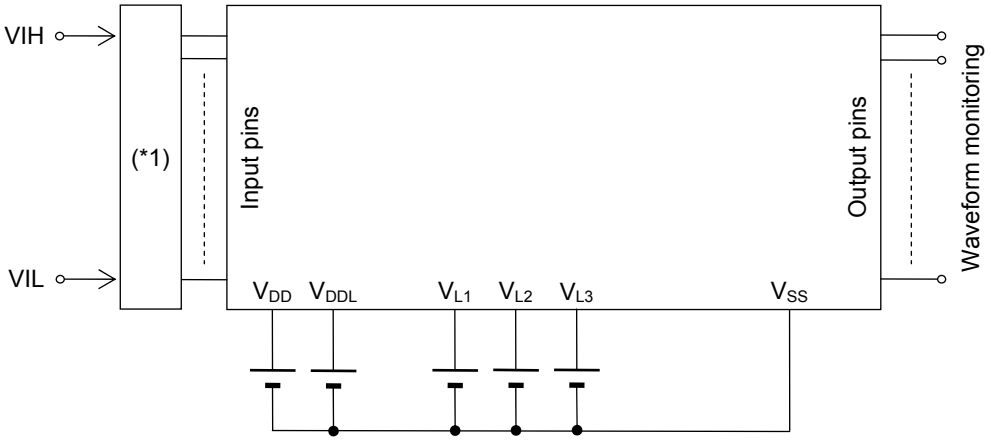
*1: Input logic circuit to determine the specified measuring conditions.
*2: Measured at the specified output pins.

MEASURING CIRCUIT 4



*3: Measured at the specified output pins.

MEASURING CIRCUIT 5

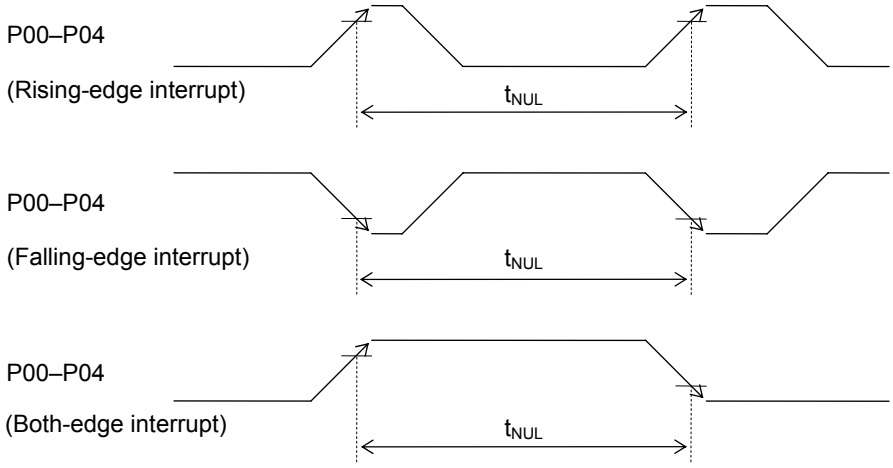


*1: Input logic circuit to determine the specified measuring conditions.

AC CHARACTERISTICS (External Interrupt)

(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation System clock: 32.768kHz	76.8	—	106.8	μs

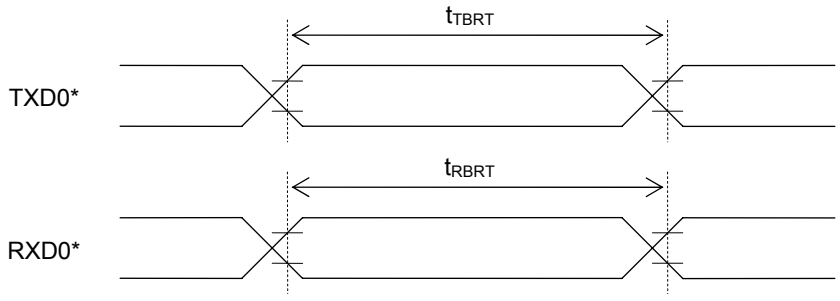


AC CHARACTERISTICS (UART)

(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Transmit baud rate	t_{TBRT}	—	—	BRT*[1]	—	s
Receive baud rate	t_{RBRT}	—	BRT*[1] –3%	BRT*[1]	BRT*[1] +3%	s

*1: Baud rate period (including the error of the clock frequency selected) set with the serial port baud rate register (SIOBRTL,H) and the serial port mode register 0 (SIOMOD0).



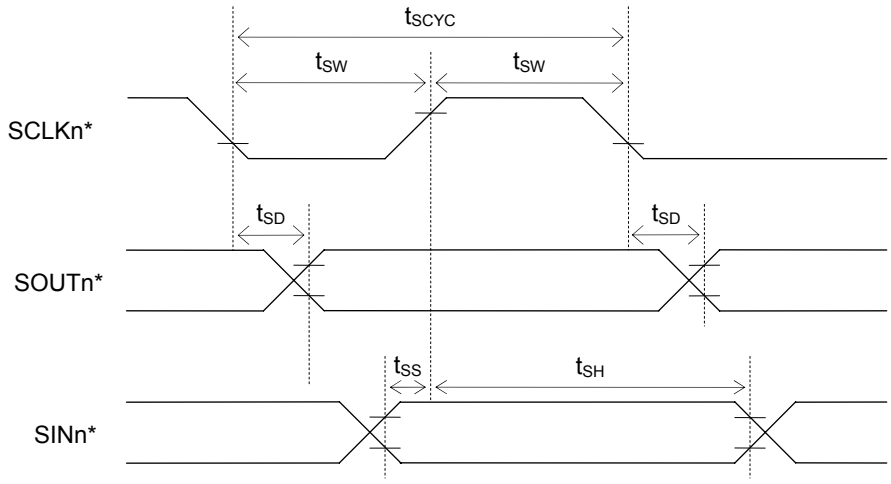
*: Indicates the secondary function of the port.

AC CHARACTERISTICS (Synchronous Serial Port)

(V_{DD}=1.25 to 3.6V, V_{SS}=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLK input cycle (slave mode)	t_{SCYC}	In the 500kHz oscillation mode*2	10	—	—	μs
		In the 2MHz oscillation mode*3 V_{DD}=1.8 to 3.6V	1	—	—	μs
SCLK output cycle (master mode)	t_{SCYC}	—	—	SCLK*1	—	s
SCLK input pulse width (slave mode)	t_{SW}	In the 500kHz oscillation mode*2	4	—	—	μs
		In the 2MHz oscillation mode*3 V_{DD}=1.8 to 3.6V	0.4	—	—	μs
SCLK output pulse width (master mode)	t_{SW}	—	SCLK*1 ×0.4	SCLK*1 ×0.5	SCLK*1 ×0.6	s
SOUT output delay time (slave mode)	t_{SD}	In the 500kHz oscillation mode*2 Output load 10pF	—	—	500	ns
		In the 2MHz oscillation mode*3 Output load 10pF	—	—	240	
SOUT output delay time (master mode)	t_{SD}	In the 500kHz oscillation mode*2 Output load 10pF	—	—	500	ns
		In the 2MHz oscillation mode*3 Output load 10pF, V_{DD}=1.8 to 3.6V	—	—	240	
SIN input setup time (slave mode)	t_{SS}	—	80	—	—	ns
SIN input setup time (master mode)	t_{SS}	In the 500kHz oscillation mode*2	500	—	—	ns
		In the 2MHz oscillation mode*3 V_{DD}=1.8 to 3.6V	240	—	—	
SIN input hold time	t_{SH}	In the 500kHz oscillation mode*2	300	—	—	ns
		In the 2MHz oscillation mode*3 V_{DD}=1.8 to 3.6V	80	—	—	

*1: Clock cycle selected with SnCK2–0 of the serial port n mode register (SIOnMOD1) (n= 0, 1)
*2: When 500kHz oscillation is selected with RCM of the frequency control register 0 (FCON0)
*3: When 2MHz oscillation is selected with RCM of the frequency control register 0 (FCON0)



*: Indicates the secondary function of the port (n= 0,1)

AC CHARACTERISTICS (RC Oscillation A/D Converter)

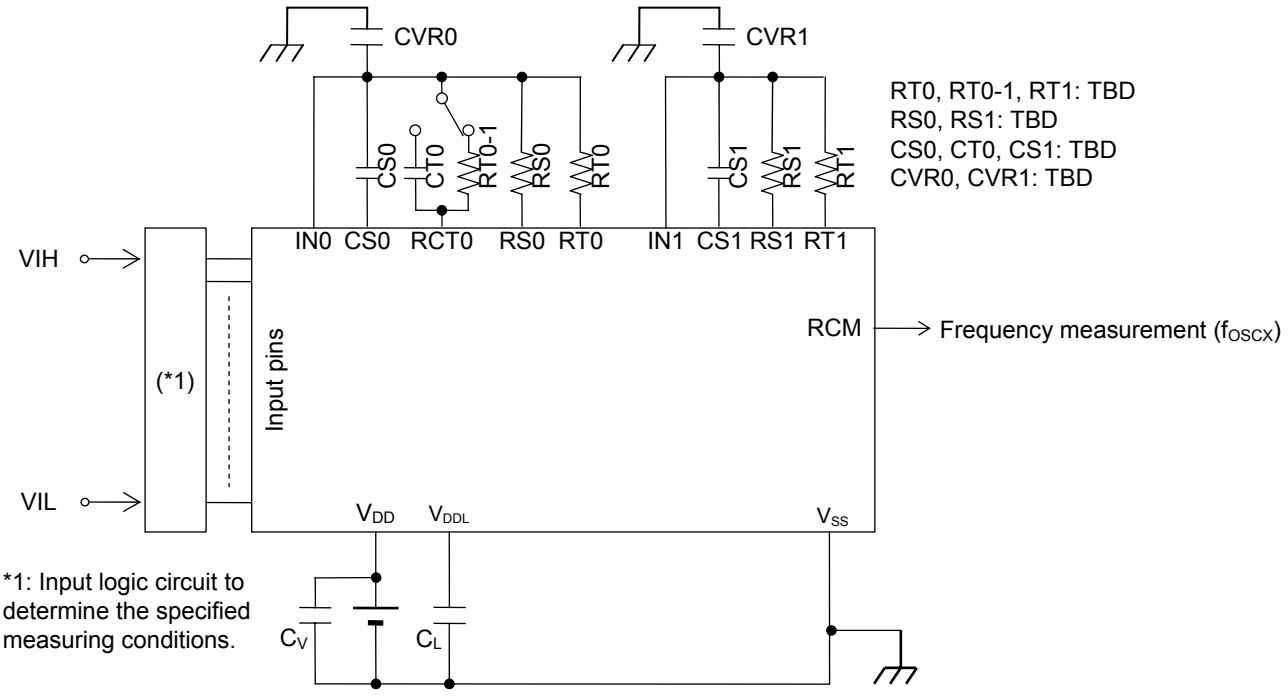
(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = −40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Resistors for oscillation	RS0, RS1, RT0, RT0-1,RT1	CS0, CT0, CS1 ≥ TBD pF	TBD	TBD	TBD	kΩ
Oscillation frequency VDD = 1.5V	f_{OSC1}	Resistor for oscillation = 1kΩ	TBD	TBD	TBD	kHz
	f_{OSC2}	Resistor for oscillation = 10kΩ	TBD	TBD	TBD	kHz
	f_{OSC3}	Resistor for oscillation = 100kΩ	TBD	TBD	TBD	kHz
RS to RT oscillation frequency ratio *1 VDD = 1.5V	Kf1	RT0, RT0-1, RT1 = 1kHz	TBD	TBD	TBD	—
	Kf2	RT0, RT0-1, RT1 = 10kHz	TBD	TBD	TBD	—
	Kf3	RT0, RT0-1, RT1 = 100kHz	TBD	TBD	TBD	—
Oscillation frequency VDD = 3.0V	f_{OSC1}	Resistor for oscillation = 1kΩ	TBD	TBD	TBD	kHz
	f_{OSC2}	Resistor for oscillation = 10kΩ	TBD	TBD	TBD	kHz
	f_{OSC3}	Resistor for oscillation = 100kΩ	TBD	TBD	TBD	kHz
RS to RT oscillation frequency ratio *1 VDD = 3.0V	Kf1	RT0, RT0-1, RT1 = 1kHz	TBD	TBD	TBD	—
	Kf2	RT0, RT0-1, RT1 = 10kHz	TBD	TBD	TBD	—
	Kf3	RT0, RT0-1, RT1 = 100kHz	TBD	TBD	TBD	—

*1: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{OSCx}(RT0\text{–}CS0\ oscillation)}{f_{OSCx}(RS0\text{–}CS0\ oscillation)}, \frac{f_{OSCx}(RT0\text{-}1\text{–}CS0\ oscillation)}{f_{OSCx}(RS0\text{–}CS0\ oscillation)}, \frac{f_{OSCx}(RT1\text{–}CS1\ oscillation)}{f_{OSCx}(RS1\text{–}CS1\ oscillation)}$$

(x = 1, 2, 3)



Note:

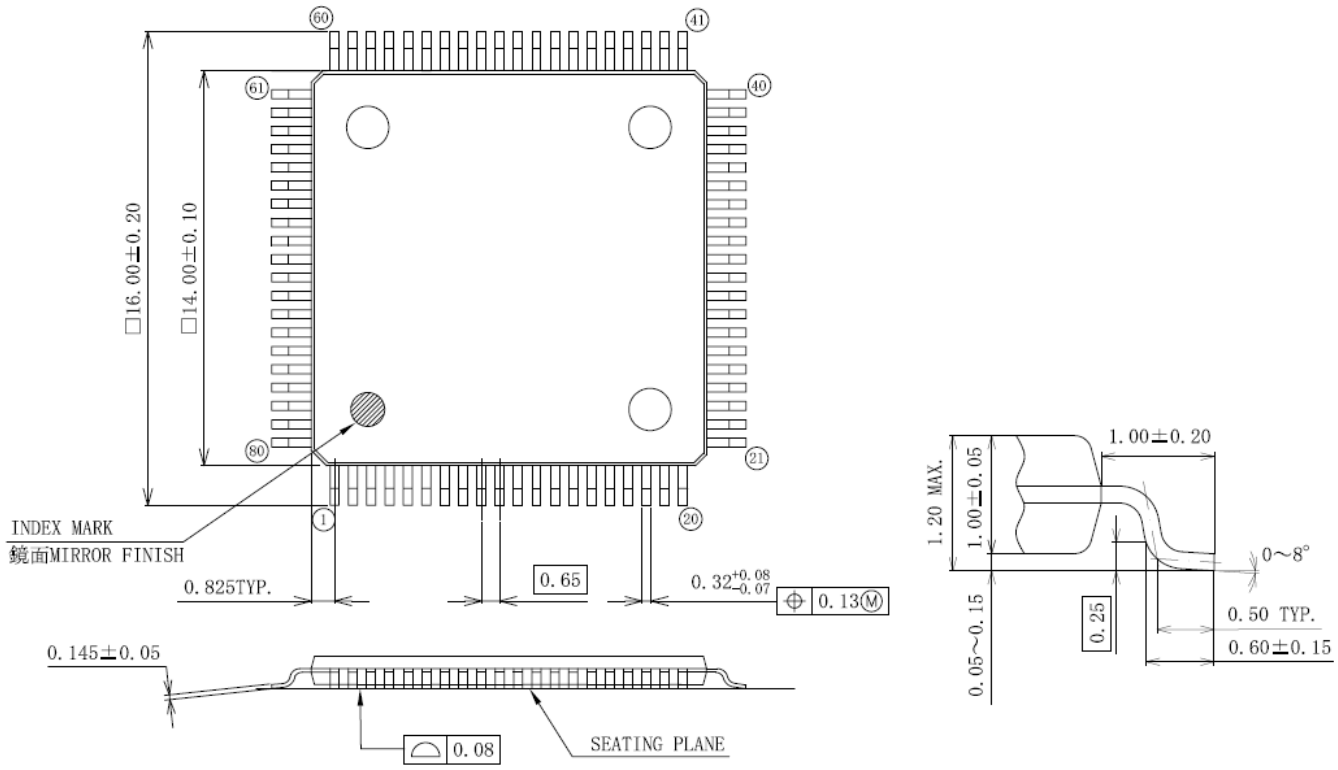
- Please have the shortest layout for the common node (wiring patterns which are connected to the external capacitors, resistors and IN0/IN1 pin), including CVR0/CVR1. Especially, do not have long wire between IN0/IN1 and RS0/RS1. The coupling capacitance on the wires may occur incorrect A/D conversion. Also, please do not have signals which may be a source of noise around the node.
- When RT0/RT1 (Thermistor and etc.) requires long wiring due to the restricted placement, please have VSS(GND) trace next to the signal.

- Please make wiring to components (capacitor, resisteor and etc.) necessory for objective measurement. Wiring to reserved components may affect to the A/D conversion operation by noise the components itself may have.

PACKAGE DIMENSIONS

(Unit: mm)

P-TQFP80-1414-0.65-ZK



OKI SEMICONDUCTOR CO., LTD.

Package material	Epoxy resin
Lead frame material	Cu alloy
Lead finish	Sn-2Bi (Bi 2%typ.)
Solder thickness	More than 5μm
Package weight (g)	0.55typ.
Rev. No./Last Revised	2 / Oct. 27,2009

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact our responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL610406-01	Jan.14,2010	–	–	Preliminary edition 1
PEDL610406-02	Jun.24,2010	1,2,4	1,2,4	Add Timer2 and Timer3
		4,8,9,10, 11,12,18, 23	4,8,9,10, 11,12,18, 23	Remove TEST1_N pin
		5,6,7	5,6,7	Add package pin layout
		12,13,14	12,13,14	Add package pin No. and change pad no.
		19 to 24	19 to 24	Fill the electrical characteristics about TBD characteristics in the first edition
		28	28	Add SSIO characteristics for 2MHz oscillation mode
		31	31	Add the package dimension

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1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

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