

**ML2282X-XXX/ML2286X-XXX****Speech Synthesis LSI with Built-in P2RPM Including 2-Channel Mixing Function****GENERAL DESCRIPTION**

The ML2282X(ML22825/ML22824/ML22823-XXX) and ML2286X(ML22865/ML22864/ML22863-XXX) are speech synthesis LSIs with built-in P2ROM that stores speech data.

These LSIs include edit ROMs, ADPCM2 decoders, 16-bit DA converters, low pass filters, and monaural speaker amplifiers.

The ML2282X supports the synchronous serial interface and the ML22865/ML22864/ML22863 support the I2C interface. By integrating all the functions required for speech output into a single chip, these LSIs can be more easily incorporated in compact portable devices.

- Built-in memory capacity and maximum vocal reproduction time:

the following table (in 4-bit OKI ADPCM2 mode)

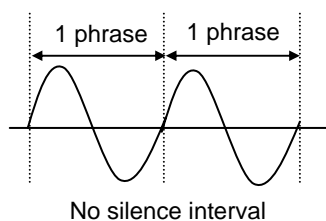
Product name	ROM capacity	Maximum vocal reproduction time (sec)		
		F _{SAM} = 4.0 kHz	F _{SAM} = 8.0 kHz	F _{SAM} = 16 kHz
ML22825-XXX/ML22865	16 Mbits	1044	522	261
ML22824-XXX/ML22864	8 Mbits	520	260	130
ML22823-XXX/ML22863	4 Mbits	258	129	64

- Speech synthesis method: 4-bit OKI ADPCM2
8-bit Nonlinear PCM
8-bit PCM/16-bit PCM
Can be specified for each phrase.
- Sampling frequency: 4.0 / 5.3 / 6.4 / 8.0 / 10.6 / 12.0 / 12.8 / 16.0 / 21.3 / 24.0 / 25.6 / 32.0 / 48.0 kHz
f_{sam} can be specified for each phrase.
- Built-in low-pass filter and 16-bit D/A converter
- Speaker driving amplifier: 0.7 W (when 8Ω, DV_{DD}=5 V, Ta=25°C)
Analog input: 2ch (internal: 1ch; external: 1ch)
- CPU command interface: 3-wired serial clock-synchronized (ML2282X)
I2C interface (ML2286X)
- Maximum number of phrases: 4096 phrases, from 000h to 3FFh (1024 phrases/bank)
- Memory bank switching: Enabled between bank 1 and bank 4 using the SEL0 and SEL1 pins
- Volume control: CVOL command can be set as 32 levels (OFF is included).
AVOL command can be set as 50 levels (OFF is included).
LOOP command
- Repeat function: Available except case using 48 kHz as sampling frequencies
- 2-channel mixing function: 4.096 MHz
- Source oscillation frequency: 2.7 to 3.6V / 4.5 to 5.5 V
- Power supply voltage: -40 to +85°C
- Operating temperature range: 30-pin plastic SSOP (SSOP30-P-56-0.65-K-MC)
- Package: ML22825-xxxMB, ML22824-xxxMB, ML22823-xxxMB
ML22865-xxxMB, ML22864-xxxMB, ML22863-xxxMB
(xxx: ROM code No.)
- Product name:

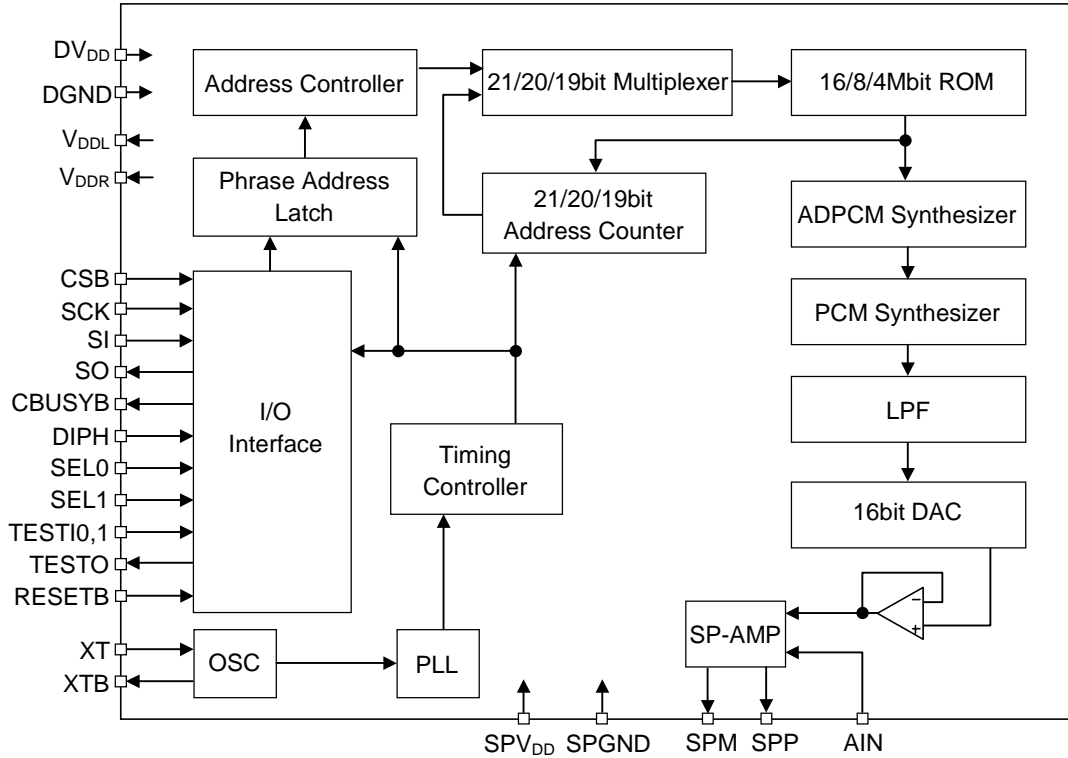
The table below summarizes the differences from the ML2216 and ML22800 series.

Parameter	ML2216	ML22800 series	ML22825/ML22824/ ML22823-XXX	ML22865/ML22864/ ML22863-XXX
CPU interface	Serial	←	←	I2C
Playback method	4-bit Oki ADPCM2 8-bit straight PCM 8-bit nonlinear PCM 16-bit straight PCM	←	←	←
Maximum number of phrases	256	1024 (256/bank)	4096 (1024/bank)	←
Sampling frequency (kHz)	4.0/5.3/6.4/ 8.0/10.6/12.8 16.0	←	4.0/5.3/6.4/8.0/ 10.6/12.0/12.8/ 16.0/21.3/24.0/ 25.6/32.0/48.0	←
Clock frequency	4.096MHz (with a built-in crystal oscillator circuit)	←	←	←
D/A converter	12 bits	12 bits	16 bits	←
Low-pass filter	3rd order comb filter	3rd order comb filter	FIR interpolation filter	←
Speaker driving amplifier	Built-in 0.3W (8Ω, DV _{DD} = 5 V)	No	Built-in 0.7W (8Ω, DV _{DD} = 5 V)	←
Edit ROM function	Yes	←	←	←
Simultaneous sound production function (mixing function)	No	←	2-channel	←
Volume control	16 levels	←	32 levels	←
Silence insertion	Yes 20 ms to 1024 ms (4 ms/step)	←	←	←
Repeat function	Yes	←	←	←
Interval at which a seam is silent during continuous playback (Note)	No	←	←	←
Memory bank switching	No	Yes	←	←
Power supply voltage	2.7 V to 5.5 V	2.7 V to 3.6 V	2.7 V to 5.5 V	←
Package	44-pin QFP	30-pin SSOP	←	←

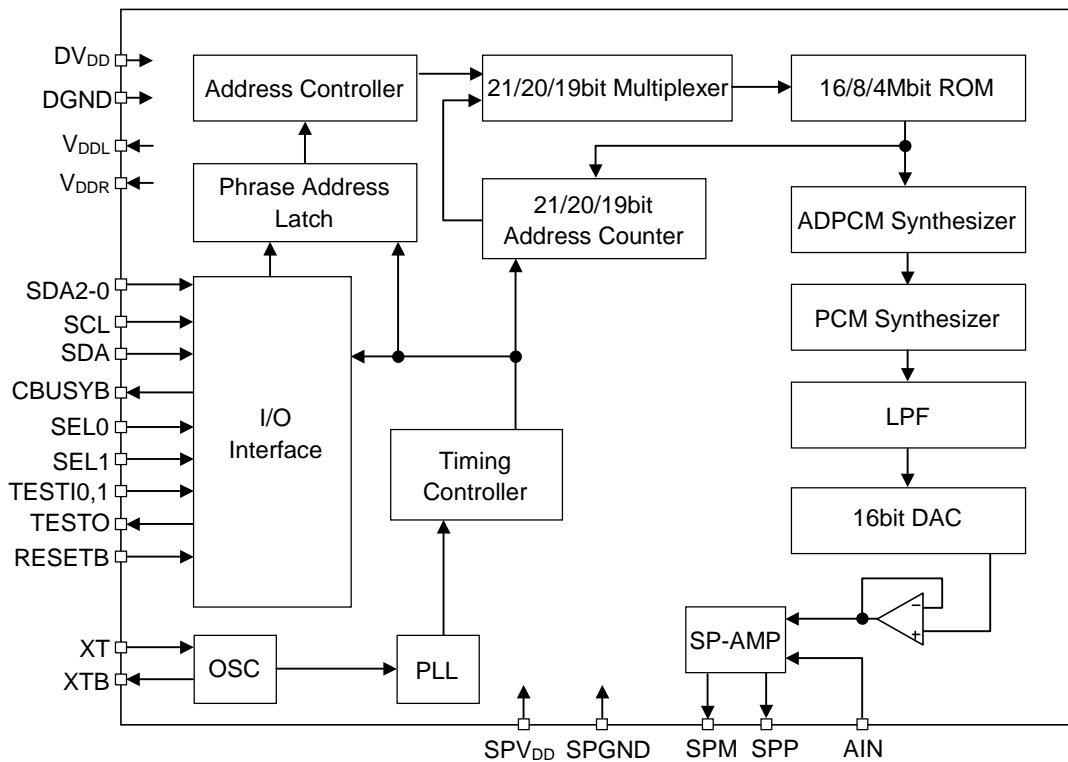
*1: Continuous playback as shown below is possible.



BLOCK DIAGRAMS
(ML22825/ML22824/ML22823-XXX)

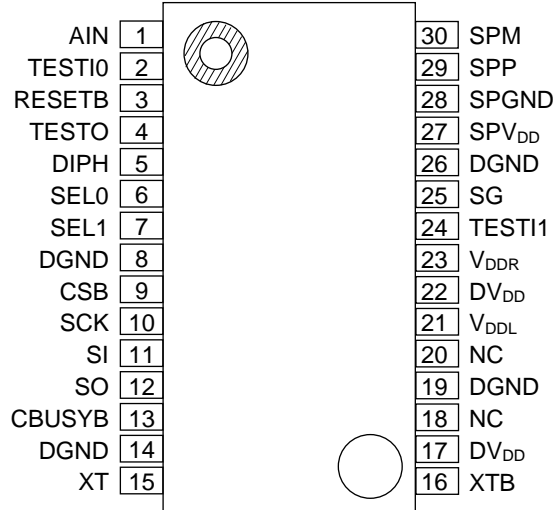


(ML22865/ML22864/ML22863-XXX)



PIN CONFIGURATIONS (TOP VIEW)

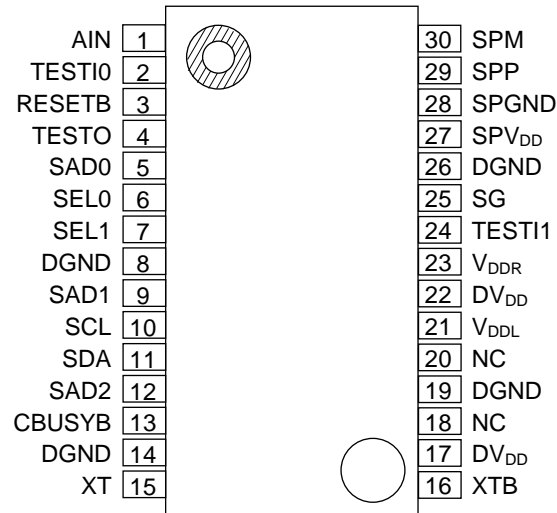
ML22825/ML22824/ML22823-XXXMB



NC: No Connection

30-Pin Plastic SSOP

ML22865/ML22864/ML22863-XXXMB



NC: No Connection

30-Pin Plastic SSOP

PIN DESCRIPTION (COMMON TO ALL PRODUCTS)

Pin	Symbol	I/O	Initial value (*1)	Description
1	AIN	I	0	Speaker amplifier input pin.
2	TESTI0	I	0	Input pin for testing. Tie this pin at a "L" level (DGND level). This pin has a pull-down resistor built in.
3	RESETB	I	0 (*2)	Reset input pin. At "L" level input, the LSI enters the initial state. During a reset input, the entire circuit is stopped and enters a power down state. Upon power-on, input a "L" level to this pin. After the power supply voltage is stabilized, drive this pin at a "H" level. By driving this pin at a "H" level, the entire circuit can be powered up. This pin has a pull-up resistor built in.
4	TESTO	O	Hi-Z	Output pin for testing. Leave this pin open.
6, 7	SEL0 SEL1	I	0	Memory bank switching pins. Fix these pins to "L" level when the memory bank function is not used.
8, 14, 19, 26	DGND	—	—	Digital ground pin. Also serves as a ground pin for the internal memory.
13	CBUSYB	O	1	Command processing status output pin. This pin outputs a "L" level during command processing. Be sure to enter commands with the CBUSYB pin driven at a "H" level.
15	XT	I	0	Connects to a crystal or a ceramic resonator. A feedback resistor of around 1 MΩ is built in between this XT pin and the XTB pin. When using an external clock, input the clock from this pin. If a crystal or a ceramic resonator is used, connect it as close to the LSI as possible.
16	XTB	O	1	Connects to a crystal or a ceramic resonator. When using an external clock, leave this pin open. If a crystal or a ceramic resonator is used, connect it as close to the LSI as possible.
17, 22	DV _{DD}	—	—	Digital power supply pin. Connect a capacitor of 0.1 μF or more between this pin and DGND.
18, 20	N.C	—	—	No-connect pins. Leave these pins open.
21	V _{DDL}	—	0	Regulator output pin for internal logic. Connect a capacitor of 10 μF or more between this pin and DGND.
23	V _{DDR}	—	0	Regulator output pin for Built-in ROM. Connect a capacitor of 10 μF or more between this pin and DGND.
24	TESTI1	—	0	Test pin. Fix this pin to a DGND level.
25	SG	—	0	Built-in speaker amplifier's reference voltage output pin. Connect a capacitor of 0.1 μF or more between this pin and DGND.
27	SPV _{DD}	—	—	Speaker amplifier power supply pin. Connect a bypass capacitor of 0.1 μF or more between this pin and SPGND.
28	SPGND	—	—	Speaker amplifier ground pin.

Pin	Symbol	I/O	Initial value (*1)	Description
29	SPP	—	0	Positive output pin of the built-in speaker amplifier. Serves as a LINE output (*3) pin if the built-in speaker amplifier is not used.
30	SPM	—	Hi-Z	Negative output pin of the built-in speaker amplifier.

*1: Indicates the initial value at reset input or during power down.

*2: “H” during power down.

*3: Outputs a voice signal before amplified by the built-in speaker amplifier.

PIN DESCRIPTION (ML2282X)

Pin	Symbol	I/O	Initial value (*1)	Description
5	DIPH	I	0	Serial interface switching pin. Pin for choosing between rising edges and falling edges as to the edges of the SCK pulses used for shifting serial data input to the SI pin into the inside of the LSI. When this pin is at a “L” level, SI input data is shifted into the LSI on the rising edges of the SCK clock pulses; when this pin is at a “H” level, SI input data is shifted into the LSI on the falling edges of the SCK clock pulses.
9	CSB	I	1	Chip select pin. A “L” level on this pin accepts the SCK or SI inputs. When this pin is at a “H” level, neither the SCK nor SI signal is input to the LSI.
10	SCK	I	1	Synchronous serial clock input pin.
11	SI	I	0	Synchronous serial data input pin. When the DIPH pin is at a “L” level, data is shifted in on the rising edges of the SCK clock pulses. When the DIPH pin is at a “H” level, data is shifted in on the falling edges of the SCK clock pulses.
12	SO	O	Hi-Z	Synchronous serial data output pin. When the DIPH pin is at a “L” level, data is output on the falling edges of the SCK clock pulses. When the DIPH pin is at a “H” level, data is output on the rising edges of the SCK clock pulses. When the CSB pin is at a “H” level, this pin goes into a Hi-Z state.

PIN DESCRIPTION (ML2286X)

Pin	Symbol	I/O	Initial value (*1)	Description
5, 9, 12	SAD0 SAD1 SAD2	I	0	Slave address select pin.
10	SCL	I	0	I2C serial clock input pin. Must be connected pull-down resistor.
11	SDA	IO	0	I2C serial data input/output pin. An input/output pin used when setting write mode/read mode, when writing addresses, and when writing or reading data. Must be connected pull-down resistor. Output: N-ch open drain output Input: High-impedance input

*1: Indicates the initial value at reset input or during power down.

ABSOLUTE MAXIMUM RATINGS

(DGND = SPGND = 0 V, Ta = 25°C)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	DV _{DD} , SPV _{DD}	—	-0.3 to +7.0	V
Input voltage	V _{IN}	—	-0.3 to DV _{DD} +0.3	V
Power dissipation	P _D		938	mW
Output short-circuit current	I _{OS}	Applies to all pins except SPM, SPP, V _{DDL} , and V _{DDR} .	10	mA
		Applies to SPM and SPP pins.	300	mA
		Applies to V _{DDL} and V _{DDR} pins.	50	mA
Storage temperature	T _{STG}	—	-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(DGND = SPGND = 0 V)

Parameter	Symbol	Condition	Range			Unit
Power supply voltage	DV _{DD} , SPV _{DD}	—	2.7 to 5.5			V
Operating temperature	T _{OP}	—	-40 to +85			°C
Master clock frequency	f _{OSC}	—	Min.	Typ.	Max.	MHz
			3.5	4.096	4.5	
External crystal oscillator	Cd, Cg	—	15	30	45	pF

ELECTRICAL CHARACTERISTICS**DC Characteristics (3 V)**DV_{DD} = SPV_{DD} = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = -40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V _{IH}	—	0.86×DV _{DD}	—	DV _{DD}	V
"L" input voltage	V _{IL}	—	0	—	0.14×DV _{DD}	V
"H" output voltage 1	V _{OH1}	I _{OH} = -1 mA	DV _{DD} -0.4	—	—	V
"H" output voltage 2 (*1)	V _{OH2}	I _{OH} = -50 μA	DV _{DD} -0.4	—	—	V
"L" output voltage 1	V _{OL1}	I _{OL} = 2 mA	—	—	0.4	V
"L" output voltage 2 (*1)	V _{OL2}	I _{OL} = 50 μA	—	—	0.4	V
"L" output voltage 3 (*2)	V _{OL3}	I _{OL} = 3 mA	—	—	0.4	V
"H" input current 1	I _{IH1}	V _{IH} = DV _{DD}	—	—	10	μA
"H" input current 2 (*3)	I _{IH2}	V _{IH} = DV _{DD}	0.3	2.0	15	μA
"H" input current 3 (*4)	I _{IH3}	V _{IH} = DV _{DD}	2	30	200	μA
"L" input current 1	I _{IL1}	V _{IL} = GND	-10	—	—	μA
"L" input current 2 (*3)	I _{IL2}	V _{IL} = GND	-15	-2.0	-0.3	μA
"L" input current 3 (*5)	I _{IL3}	V _{IL} = GND	-200	-30	-2	μA
"H" output leak current 3 (*6)	I _{ILOH}	V _{OH} = DV _{DD}	—	—	10	μA
"L" output leak current 3 (*6)	I _{ILOL}	V _{OL} = GND	-10	—	—	μA
Supply current during playback	I _{DD}	f _{OSC} = 4.096 MHz No output load	—	—	20	mA
Power-down supply current	I _{DDS}	Ta = -40 to +40°C	—	1	10	μA
		Ta = -40 to +85°C	—	1	20	μA

*1: Applies to the XTB pin.

*2: Applies to the SCL, SDA pin.

*3: Applies to the XT pin.

*4: Applies to the TESTI0 pin.

*5: Applies to the RESETB pin.

*6: Applies to the TESTO pin.

DC Characteristics (5 V) $DV_{DD} = SPV_{DD} = 4.5$ to 5.5 V, $DGND = SPGND = 0$ V, $T_a = -40$ to $+85^\circ\text{C}$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	$0.8 \times DV_{DD}$	—	DV_{DD}	V
"L" input voltage	V_{IL}	—	0	—	$0.2 \times DV_{DD}$	V
"H" output voltage 1	V_{OH1}	$I_{OH} = -1$ mA	$DV_{DD} - 0.4$	—	—	V
"H" output voltage 2 (*1)	V_{OH2}	$I_{OH} = -50$ μA	$DV_{DD} - 0.4$	—	—	V
"L" output voltage 1	V_{OL1}	$I_{OL} = 2$ mA	—	—	0.4	V
"L" output voltage 2 (*1)	V_{OL2}	$I_{OL} = 50$ μA	—	—	0.4	V
"L" output voltage 3 (*2)	V_{OL3}	$I_{OL} = 3$ mA	—	—	0.4	V
"H" input current 1	I_{IH1}	$V_{IH} = DV_{DD}$	—	—	10	μA
"H" input current 2 (*3)	I_{IH2}	$V_{IH} = DV_{DD}$	0.8	5.0	20	μA
"H" input current 3 (*4)	I_{IH3}	$V_{IH} = DV_{DD}$	20	100	400	μA
"L" input current 1	I_{IL1}	$V_{IL} = \text{GND}$	-10	—	—	μA
"L" input current 2 (*3)	I_{IL2}	$V_{IL} = \text{GND}$	-20	-5.0	-0.8	μA
"L" input current 3 (*5)	I_{IL3}	$V_{IL} = \text{GND}$	-400	-100	-20	μA
"L" output leak current 2 (*6)	I_{ILOH}	$V_{OH} = DV_{DD}$	—	—	10	μA
"L" output leak current 3 (*6)	I_{ILOL}	$V_{OL} = \text{GND}$	-10	—	—	μA
Supply current during playback	I_{DD}	$f_{OSC} = 4.096$ MHz No output load	—	—	25	mA
Power-down supply current	I_{DDS}	$T_a = -20$ to $+40^\circ\text{C}$	—	1	15	μA
		$T_a = -20$ to $+85^\circ\text{C}$	—	1	30	μA

*1: Applies to the XTB pin.

*2: Applies to the SCL, SDA pin.

*3: Applies to the XT pin.

*4: Applies to the TESTI0 pin.

*5: Applies to the RESETB pin.

*6: Applies to the TESTO pin.

Analog Section Characteristics (3 V) $DV_{DD} = SPV_{DD} = 2.7$ to 3.6 V, $DGND = SPGND = 0$ V, $T_a = -40$ to $+85^\circ\text{C}$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AIN input resistance	R_{AIN}	—	15	20	25	$k\Omega$
AIN input voltage range	V_{AIN}	—	—	—	$DV_{DD} \times 2/3$	Vp-p
LINE output load resistance	R_{LA}	During 1/2 DV_{DD} output	10	—	—	$k\Omega$
LINE output voltage range	V_{AO}	No output load	$DV_{DD}/6$	—	$DV_{DD} \times 4/6$	V
SG output voltage	V_{SG}	—	$0.95 \times V_{DDL}/2$	$V_{DDL}/2$	$1.05 \times V_{DDL}/2$	V
SG output resistance	R_{SG}	During power down	52	96	135	$k\Omega$
SPM, SPP output load resistance	R_{LSP}	—	8	—	—	Ω
Speaker amplifier output power	P_{SPO}	$SPV_{DD} = 3.3\text{V}$, $f = 1\text{kHz}$ $R_{SPO} = 8\Omega$, $THD \geq 10\%$	100	300	—	mW
Output offset voltage between SPM and SPP with no signal present	V_{OF}	SPIN–SPM gain = 0dB With a load of 8Ω	–50	—	+50	mV

Analog Section Characteristics (5 V) $DV_{DD} = SPV_{DD} = 4.5$ to 5.5 V, $DGND = SPGND = 0$ V, $T_a = -20$ to $+85^\circ\text{C}$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AIN input resistance	R_{AIN}	—	15	20	25	$k\Omega$
AIN input voltage range	V_{AIN}	—	—	—	$DV_{DD} \times 2/4$	Vp-p
LINE output load resistance	R_{LA}	During 1/2 DV_{DD} output	10	—	—	$k\Omega$
LINE output voltage range	V_{AO}	No output load	$DV_{DD}/6$	—	$DV_{DD} \times 4/6$	V
SG output voltage	V_{SG}	—	$0.95 \times V_{DDL}/2$	$V_{DDL}/2$	$1.05 \times V_{DDL}/2$	V
SG output resistance	R_{SG}	During power down	57	96	135	$k\Omega$
SPM, SPP output load resistance	R_{LSP}	—	8	—	—	Ω
Speaker amplifier output power	P_{SPO}	$SPV_{DD} = 5.0\text{V}$, $f = 1\text{kHz}$ $R_{SPO} = 8\Omega$, $THD \geq 10\%$ $T_a = 25^\circ\text{C}$	500	700	—	mW
Output offset voltage between SPM and SPP with no signal present	V_{OF}	SPIN–SPM gain = 0dB With a load of 8Ω	–50	—	+50	mV

AC Characteristics (Common to All Products)
 $DV_{DD} = SPV_{DD} = 2.7 \text{ to } 5.5 \text{ V}$, $DGND = SPGND = 0 \text{ V}$, $T_a = -40 \text{ to } +85^\circ\text{C}$, Load capacitance = 45 pF

Parameter	Applicable command	Symbol	Condition	Min.	Typ.	Max.	Unit
Master clock duty cycle		f_{duty}	—	40	50	60	%
RESETB input pulse width		t_{RST}	—	100	—	—	μs
Reset noise rejection pulse width		t_{NRST}	—	—	—	0.1	μs
Command input interval time	STOP, SLOOP, CLOOP, CVOL, AVOL	t_{INT}	$f_{OSC} = 4.096 \text{ MHz}$	2	—	—	ms
	PUP	t_{INTP}		10	—	—	ms
	RDSTAT	t_{INTRD}		500	—	—	μs
Command input enable time	SLOOP (during continuous playback)	t_{cm}	$f_{OSC} = 4.096 \text{ MHz}$	—	—	10	ms
CBUSYB "L" level output time	PUP	t_{PUP1}	$f_{OSC} = 4.096 \text{ MHz}$ When an external clock is input	—	—	10	ms
	PDWN	t_{PD1}	$f_{OSC} = 4.096 \text{ MHz}$	—	—	20	μs
	AMODE (PUP = "0" DAEN (or SPEN) = "L" → "H")	t_{PUPA1}	$f_{OSC} = 4.096 \text{ MHz}$ When an external clock is input	58	60	62	ms
	AMODE (PUP = "1" DAEN (or SPEN) = "L" → "H")	t_{PUPA2}	$f_{OSC} = 4.096 \text{ MHz}$ When an external clock is input	90	93	95	ms
	AMODE (PUP = "0" DAEN (or SPEN) = "H" → "L")	t_{PDA1}	$f_{OSC} = 4.096 \text{ MHz}$ When an external clock is input	108	110	112	ms
	AMODE (PUP = "1" DAEN (or SPEN) = "H" → "L")	t_{PDA2}	$f_{OSC} = 4.096 \text{ MHz}$ When an external clock is input	140	142	144	ms
CBUSYB "L" level output time 1(*1)		t_{CB1}	$f_{OSC} = 4.096 \text{ MHz}$	—	—	2	μs

Note: Output pin load capacitance = 45 pF

*1: Applies to cases where a command is input except after a PUP, PDWN, or AMODE command input.

AC Characteristics (ML2282X)
 $DV_{DD} = SPV_{DD} = 2.7 \text{ to } 5.5 \text{ V}$, $DGND = SPGND = 0 \text{ V}$, $T_a = -40 \text{ to } +85^\circ\text{C}$, Load capacitance = 45 pF

Parameter	Applicable command	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK input enable time from CSB fall		t_{ESCK}	—	100	—	—	Ns
SCK hold time from CSB rise		t_{CSH}	—	100	—	—	ns
Data floating time from CSB rise		t_{DOZ}	$R_L = 3 \text{ k}\Omega$	—	—	100	ns
Data setup time from SCK rise		t_{DIS1}	DIPH = "L"	50	—	—	ns
Data hold time from SCK rise		t_{DIH1}	DIPH = "L"	50	—	—	ns
Data output delay time from SCK rise		t_{DOD1}	$R_L = 3 \text{ k}\Omega$	—	—	80	ns
Data setup time from SCK fall		t_{DIS2}	DIPH = "H"	50	—	—	ns
Data hold time from SCK fall		t_{DIH2}	DIPH = "H"	50	—	—	ns
Data output delay time from SCK rise		t_{DOD2}	$R_L = 3 \text{ k}\Omega$	—	—	80	ns
SCK "H" level pulse width		t_{SCKH}	—	100	—	—	ns
SCK "L" level pulse width		t_{SCKL}	—	100	—	—	ns
CBUSYB output delay time from SCK rise		t_{DBSY1}	DIPH = "L"	—	—	150	ns
CBUSYB output delay time from SCK fall		t_{DBSY2}	DIPH = "H"	—	—	150	ns

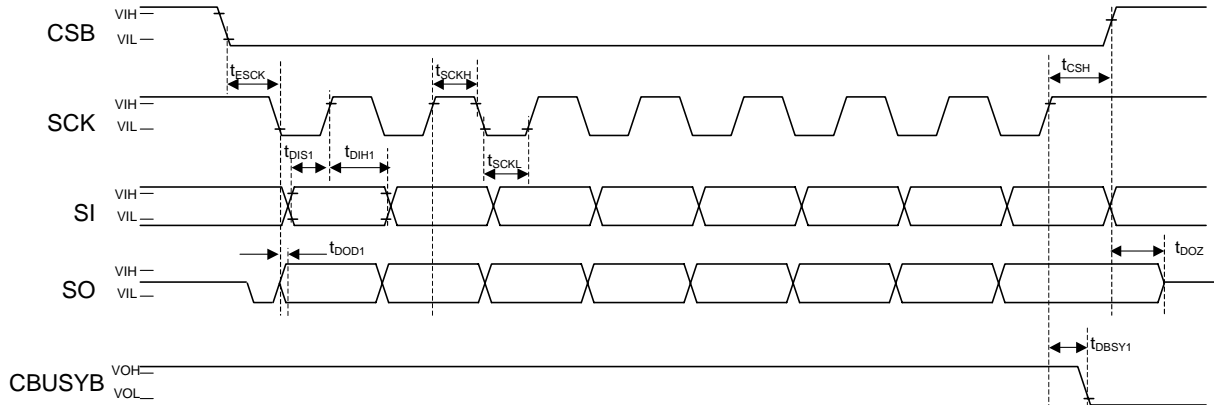
Note: Output pin load capacitance = 45 pF

AC Characteristics (ML2286X)DV_{DD} = SPV_{DD} = 2.7 to 5.5 V, DGND = SPGND = 0 V, Ta = -40 to +70°C

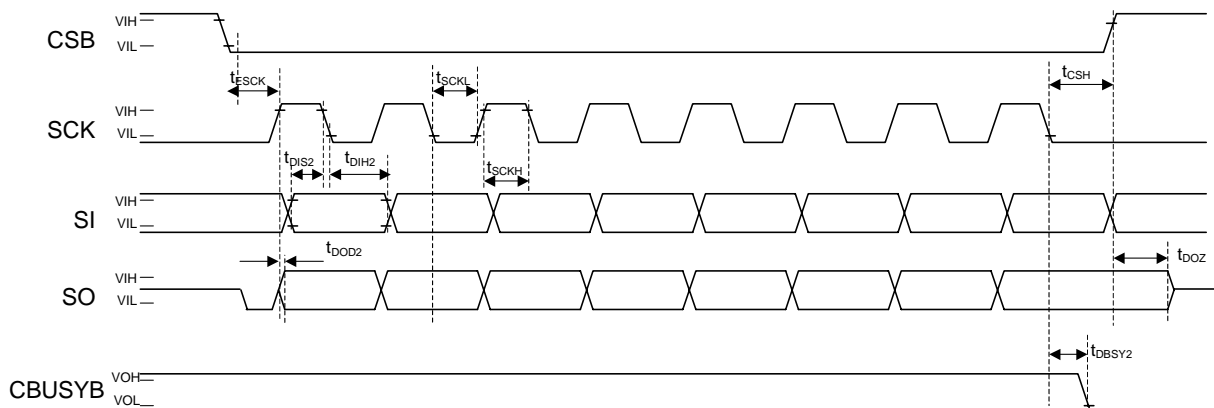
Parameter	Symbol	(High-speed mode)		Unit
		Min.	Max.	
SCL clock frequency	t _{SCL}	0	400	kHz
Hold time (repeated) START condition After this period, the first clock pulse is generated.	t _{HD;STA}	0.6	—	μs
“L” level pulse width of SCL clock	t _{LOW}	1.3	—	μs
“H” level pulse width of SCL clock	t _{HIGH}	0.6	—	μs
Repeated START condition setup time	t _{SU;STA}	0.6	—	μs
Data hold time: For I2C bus devices	t _{HD;DAT}	0	0.9	μs
Data setup time	t _{SU;DAT}	100	—	ns
SDA and SCL signal rise time	t _r	20	300	ns
SDA and SCL signal fall time	t _f	20	300	ns
STOP condition setup time	t _{SU;STO}	0.6	—	μs
Bus free time between STOP condition and START condition	t _{BUF}	1.3	—	μs
Capacitive load for each bus line	C _b	—	400	PF
Noise margin at a “L” level in each device connected (including hysteresis)	V _{nL}	0.1× DV _{DD}	—	V
Noise margin at a “H” level in each device connected (including hysteresis)	V _{nH}	0.1× DV _{DD}	—	V

TIMING DIAGRAMS

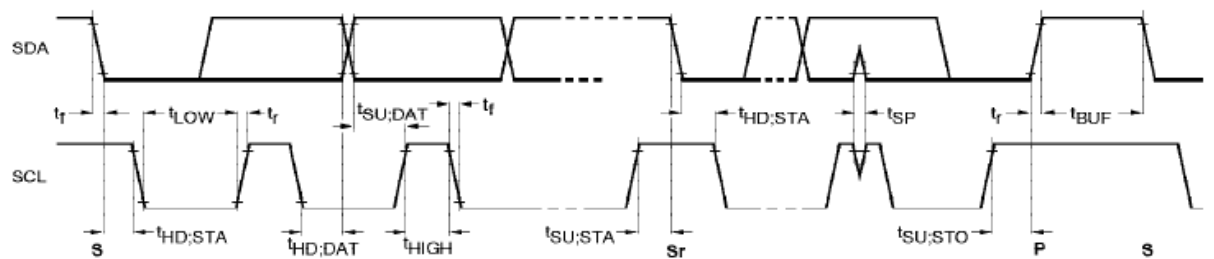
Serial CPU Interface Timing (When DIPH = "L")



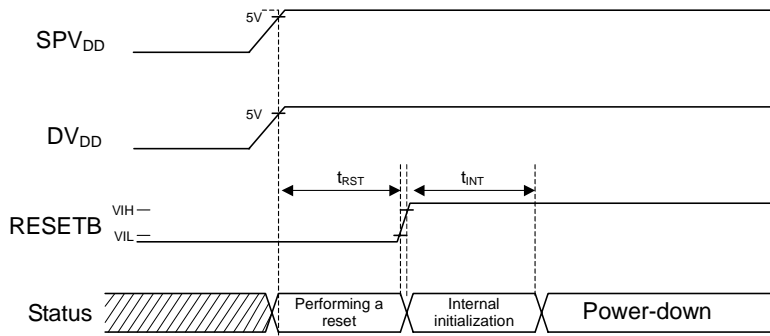
Serial CPU Interface Timing (When DIPH = "H")



I2C Interface Timing (for ML2286X)

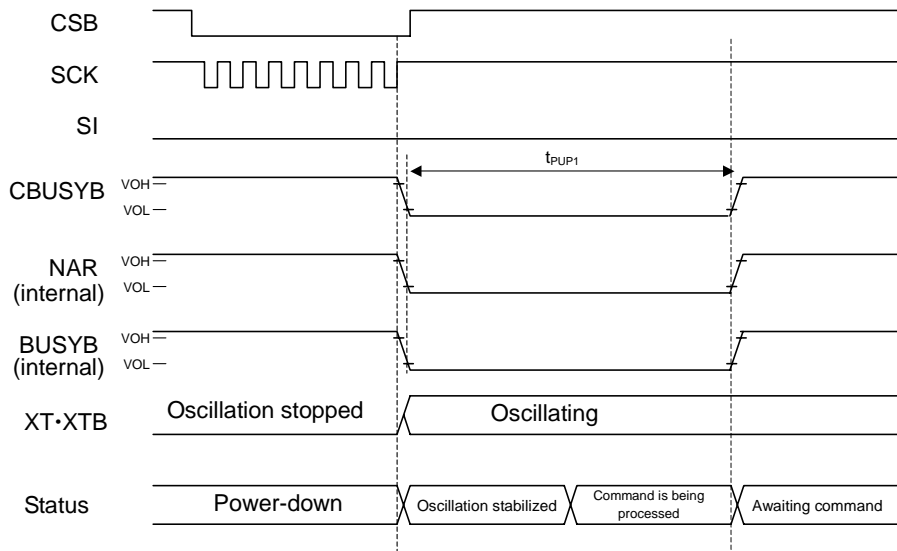


Power-On Timing

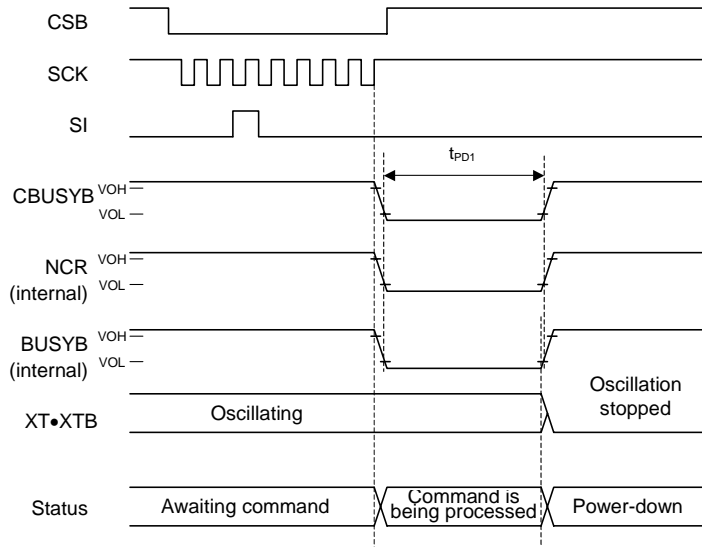


Oscillation is stopped after power-on.

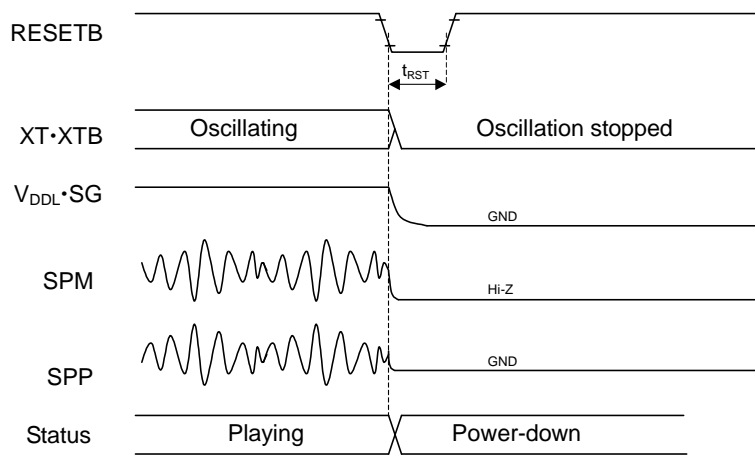
Power-Up Timing



Power-Down Timing

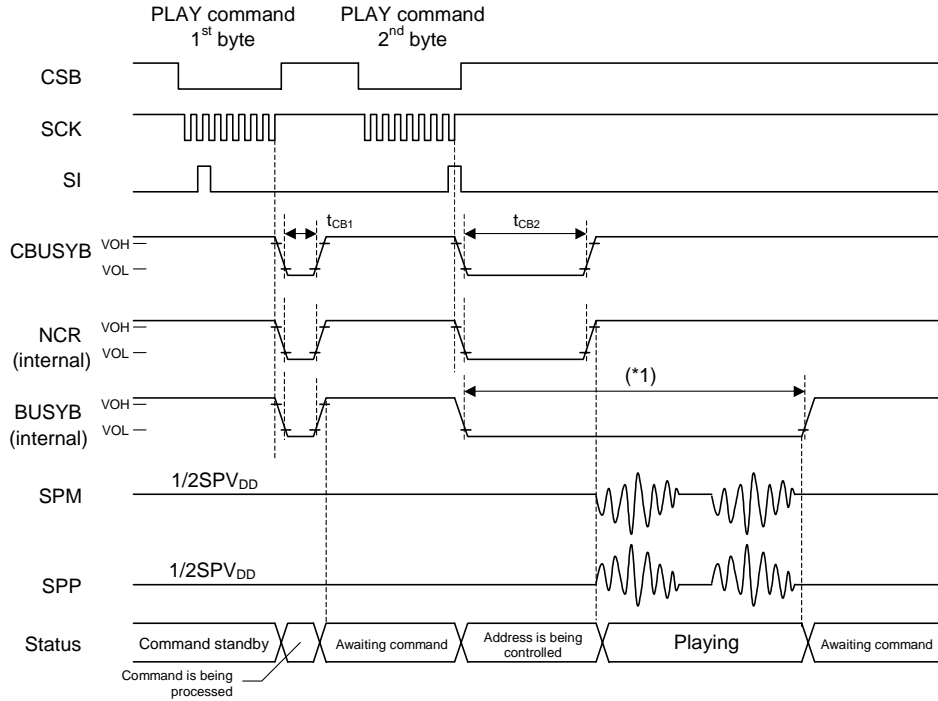


At RESET input



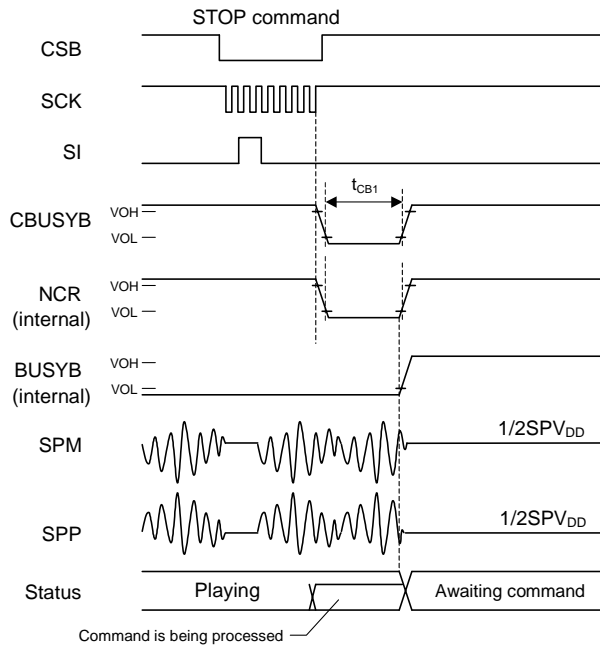
Note: The same timing applies in cases where the RESETB signal is input during command waiting.

Playback Start Timing by the PLAY Command

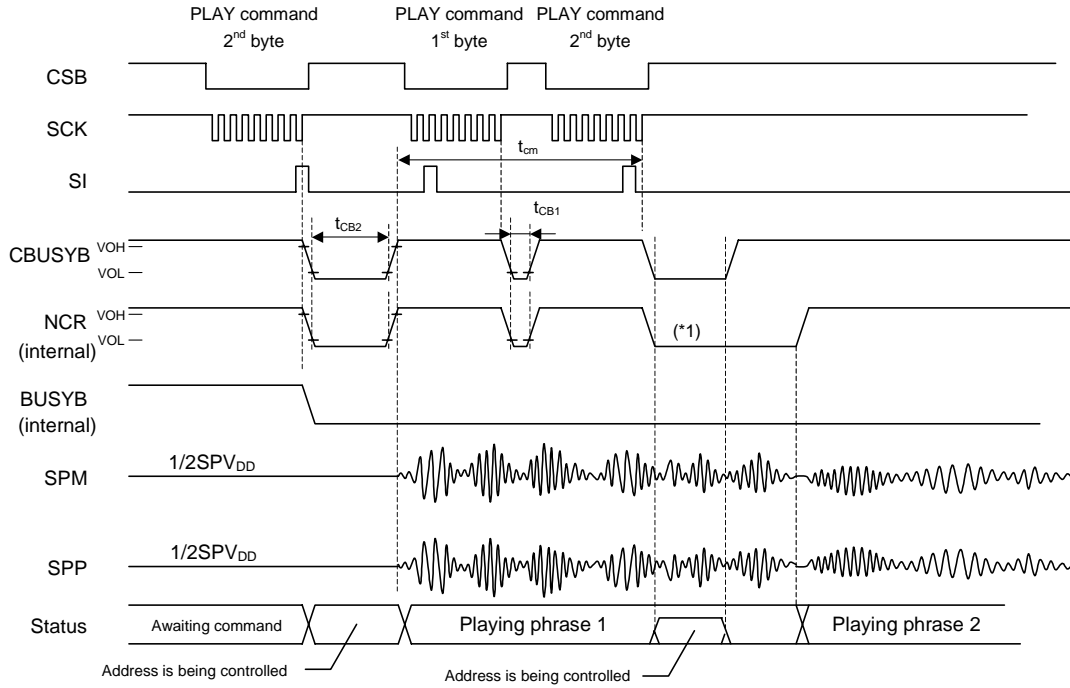


Note: The length of the “L” interval of BUSYB is t_{CB1} + voice reproduction time.

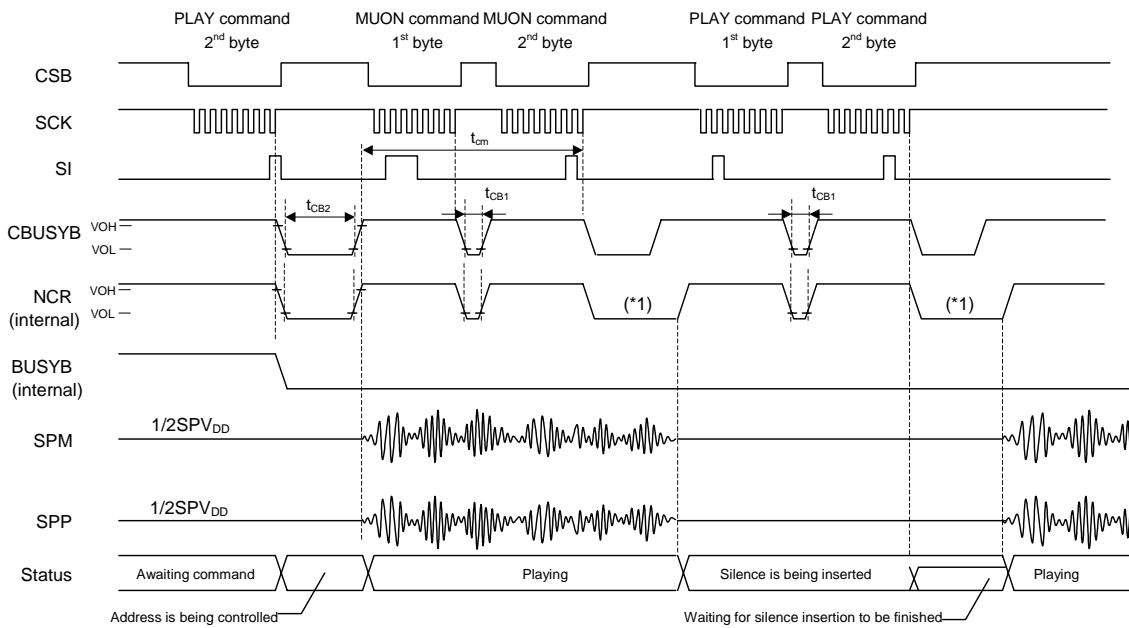
Playback Stop Timing



Continuous Playback Timing by the PLAY Command

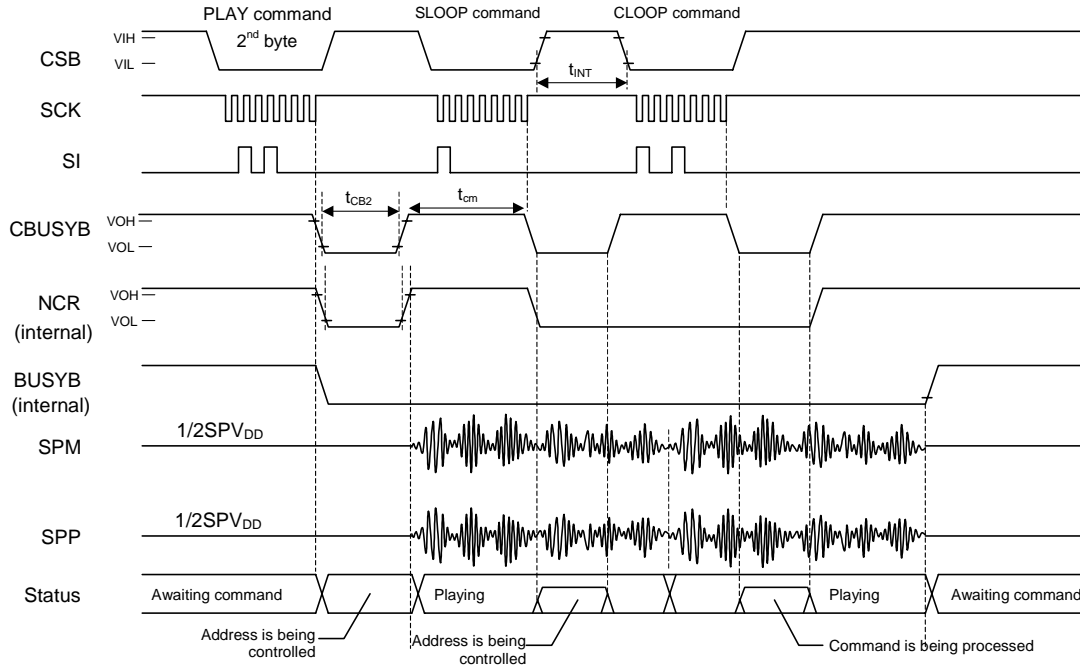


Silence Insertion Timing by the MUON Command

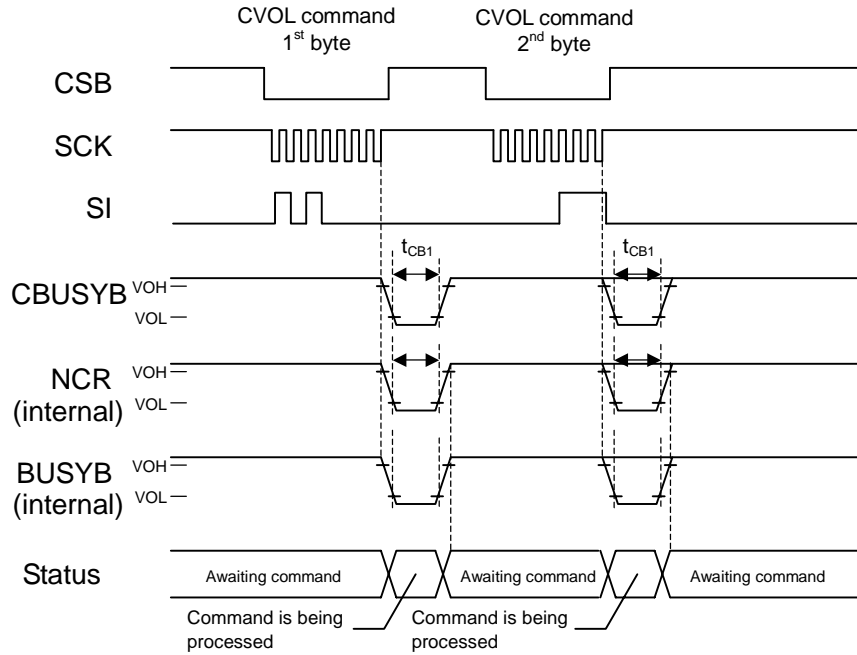


*1: The “L” level period of the NCR signal during playback or silence insertion operation varies depending on the timing on which the MUON command is input.

Repeat Playback Set/Release Timing by the SLOOP and CLOOP Commands



Timing of Volume Change by the CVOL Command



FUNCTIONAL DESCRIPTION

• Synchronous Serial Interface

The CSB, SCK, SI, and SO pins are used to input various commands and data or read the status of the ML2272X/ML2276X. Driving the CSB pin at a “L” level enables the serial CPU interface.

After the CSB pin is driven “L”, command and data are input through the SI pin from the MSB in synchronization with the SCK clock signal. Next, the data input through the SI pin is shifted into the LSI on the rising or falling edges of the SCK clock pulses. Then, a command is executed at the rising or falling edge of the eighth pulse of the SCK clock.

As for status reading, status is output from the SO pin in sync with the SCK clock signal after a “L” level is input to the CSB pin.

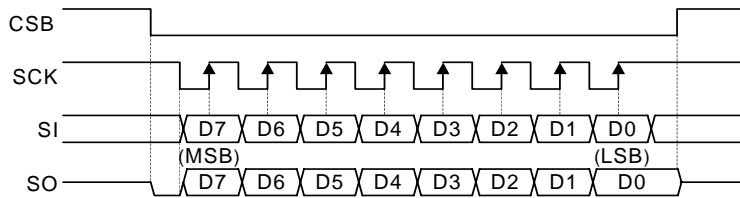
Choosing between rising edges and falling edges of the clock pulses input through the SCK pin is determined by the signal input through the DIPH pin:

- When the DIPH pin is at a “L” level, the data input through the SI pin is shifted into the LSI on the rising edges of the SCK clock pulses.
- When the DIPH pin is at a “H” level, the data input through the SI pin is shifted into the LSI on the falling edges of the SCK clock pulses.

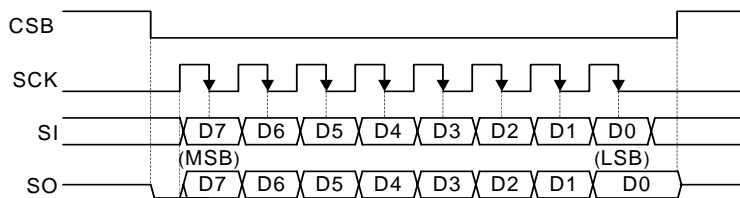
It is possible to input command and data in the LSI even by tying the CSB pin to a “L” level. However, if unexpected pulses caused by noise are induced through the SCK pin, SCK clock pulses are incorrectly counted, causing a failure in normal recognition of command. Driving the CSB pin at a “H” level returns the count of the SCK clock pulses to the initial state.

Command and Data Input Timing

- SCK rising edge operation (when DIPH pin = “L” level)



- SCK falling edge operation (when DIPH pin = “H” level)



The table below shows the contents of each data output at a status read.

	Output status signal
MSB	—
7SB	—
6SB	Channel 2 BUSYB output (BUSYB1)
5SB	Channel 1 BUSYB output (BUSYB0)
4SB	—
3SB	—
2SB	Channel 2 NCR output (NCR1)
LSB	Channel 1 NCR output (NCR0)

The BUSYB signal outputs a “L” level when a command is being processed and/or the playback of a particular channel is going on. In other states, the BUSYB signal outputs a “H” level. The NCR signal outputs a “L” level when a command is being processed and/or particular channel is in standby for playback. In other states, the NCR signal outputs a “H” level.

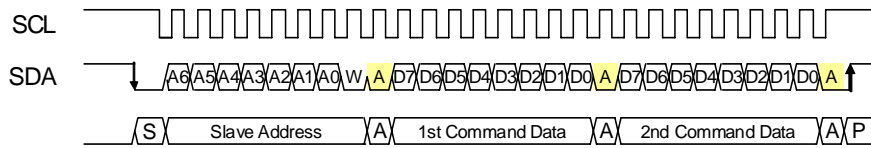
• I2C Interface (Applies to ML2286X)

The I2C Interface is an interface (slave) that is compliant with I2C bus specification. It supports Fast mode and enables data transmission/reception at 400 kbps. The SCL and SDA pins are used to input various commands and data or read the status of the ML2286X. SAD0–2 pins are used to set a slave address.

For the master on the I2C bus to communicate with the ML2286X, input the slave address of the ML2286X with the first seven bits after a START condition. In the ML2286X, the upper three bits of a slave address can be set using the SAD0–2 pins. Next, determine the communication direction with the eighth bit: if the eighth bit is “0”, it indicates that data is written from the master and if it is “1”, it indicates that data is read from the master. From this onward, communication is made in units of bytes. In this case, each byte is required to be acknowledged. Use the protocols shown below to make I2C communication.

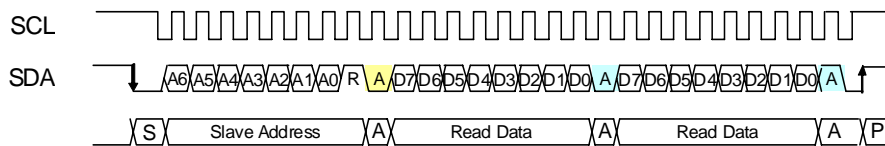
- Command flow at data write
 - START condition
 - Slave address +W (0)
 - Write address (ex. 1st byte of a command)
 - Write data (ex. 2nd byte of a command)
 - STOP condition

• Data write timing



- Command flow at data read
 - START condition
 - Slave address +W (0)
 - Read address (ex. RDSTAT command)
 - START condition
 - Slave address +R (1) (ex. RDSTAT command)
 - Read data (ex. Status read)

• Data read timing



Use the SAD0–2 pins to set a slave address as follows:

SAD2	SAD1	SAD0	Lower 4 bits
0	0	0	0101
0	0	1	0101
0	1	0	0101
0	1	1	0101
1	0	0	0101
1	0	1	0101
1	1	0	0101
1	1	1	0101

The table below shows the contents of each data output at a status read. Status is updated by the RDSTAT command; therefore, in order to read status, be sure to input the RDSTAT command.

ML228XX

	Output status signal
MSB	
7SB	
6SB	Channel 1 BUSYB output (BUSYB1)
5SB	Channel 0 BUSYB output (BUSYB0)
4SB	
3SB	
2SB	Channel 1 NCR output (NCR1)
LSB	Channel 0 NCR output (NCR0)

The BUSYB signal outputs a “L” level when either a command is being processed or the playback of a particular channel is going on. In other states, the BUSYB signal outputs a “H” level. The NCR signal outputs a “L” level when either a command is being processed or a particular channel is in standby for playback. In other states, the NCR signal outputs a “H” level.

• Command List

Each command is configured in 1-byte (8-bit) units. Each of the AMODE, AVOL FADR, PLAY, MUON, and CVOL, commands forms one command by two bytes.

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
PUP	0	0	0	0	0	0	S1	S0	Power-up command. Shifts the device currently powered down to a command wait state. Also, sets the number of memory banks.
PDWN	0	0	1	0	0	0	0	0	Power-down command. Shifts the device from a command wait state to a power-down state.
RDSTAT	1	0	1	1	0	0	0	0	Command status read command. Reads the command status on each channel.
AMODE	0	0	0	0	0	1	0	0	Analog section control command. Configures settings for power-up operation and analog input/output.
	FAD	DAG1	DAG0	AIG1	AIG0	DAEN	SPEN	PUP	
PLAY	0	1	0	0	F9	F8	0	CH	Playback start command. Use the data of the 2nd byte to specify a phrase number. Can be specified for each channel.
	F7	F6	F5	F4	F3	F2	F1	F0	
STOP	0	1	1	0	0	0	CH1	CH0	Playback stop command. Can be specified for each channel.
FADR	0	0	1	1	F9	F8	0	CH	Playback phrase specification command. Can be specified for each channel.
	F7	F6	F5	F4	F3	F2	F1	F0	
START	0	1	0	1	0	0	CH1	CH0	Playback start command without phrase specification. Used to start playback on multiple channels at the same time after phrases are specified with the FADR command. After a phrase is played with the PLAY command, the same phrase can be played with this command.
MUON	0	1	1	1	0	0	CH1	CH0	Silence insertion command. Use the data of the 2nd byte to specify the length of silence. Can be specified for each channel.
	M7	M6	M5	M4	M3	M2	M1	M0	
SLOOP	1	0	0	0	0	0	CH1	CH0	Repeat playback setting command. The setting is enabled during playback. Can be specified for each channel.
CLOOP	1	0	0	1	0	0	CH1	CH0	Repeat playback cancellation command. When the STOP command is input, repeat playback mode is released automatically. Can be specified for each channel.
CVOL	1	0	1	0	0	0	CH1	CH0	Volume setting command. Use the data of the 2nd byte to specify volume. Can be specified for each channel.
	0	0	0	CV4	CV3	CV2	CV1	CV0	

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
AVOL	0	0	0	0	1	0	0	0	Analog volume setting command.
	0	0	AV5	AV4	AV3	AV2	AV1	AV0	Use the data of the 2nd byte to specify volume.

• **Voice Synthesis Algorithm**

The ML2272X/ML2276X contain four algorithm types to match the characteristic of playback voice: 4-bit ADPCM2 algorithm, 8-bit straight ADPCM2 algorithm, 8-bit non-linear PCM algorithm, and 16-bit straight PCM algorithm.

Key feature of each algorithm is described in the table below.

Voice synthesis algorithm	Applied waveform	Feature
OKI 4-bit ADPCM2	Normal voice waveform	OKI's specific speech synthesis algorithm of improved waveform follow-up with improved 4-bit ADPCM.
OKI 8-bit Nonlinear PCM	High-frequency components inclusive sound effect etc.	Algorithm, which plays back mid-range of waveform as 10-bit equivalent voice quality.
8-bit PCM		Normal 8-bit PCM algorithm
16-bit PCM		Normal 16-bit PCM algorithm

• Memory Allocation and Creating Voice Data

The ROM is partitioned into four data areas: voice (i.e., phrase) control area, test area, voice area, and edit ROM area.

The voice control area manages the ROM's voice data. It contains data for controlling the start/stop addresses of voice data for 1024 phrases, use/non-use of the edit ROM function and so on.

The test area contains data for testing.

The voice area contains actual waveform data.

The edit ROM area contains data for effective use of voice data. For the details, refer to the section of "Edit ROM Function."

No edit ROM area is available unless the edit ROM is used.

The ROM data is created using a dedicated tool.

Configuration of ROM data

0x00000	Voice control area (Fixed 64 Kbits)
0x01FFF	
0x02000	Test area
0x0205F	
0x02060	Voice area
max: 0xFFFFF	
max: 0xFFFFF	
max: 0xFFFFF	Edit ROM area Depends on creation of ROM data.

• Playback Time and Memory Capacity

The playback time depends on the memory capacity, sampling frequency, and playback method.

The equation showing the relationship is given below.

The equation below gives the playback time when the edit ROM function is not used.

$$\text{Playback time [sec]} = \frac{1.024 \times (\text{Memory capacity} - 64) \text{ [Kbits]}}{\text{Sampling frequency [kHz]} \times \text{Bit length}}$$

where the bit length is 4 bits for 4-bit ADPCM2 and 8 or 16 bits for PCM.

Example: Let the sampling frequency be 16 kHz and 4-bit ADPCM2 algorithm. Then the playback time is approx. 261 seconds, as shown below.

$$\text{Playback time} = \frac{1.024 \times (16834 - 64) \text{ [Kbits]}}{16 \text{ [kHz]} \times 4 \text{ [bits]}} \cong 261 \text{ [sec]}$$

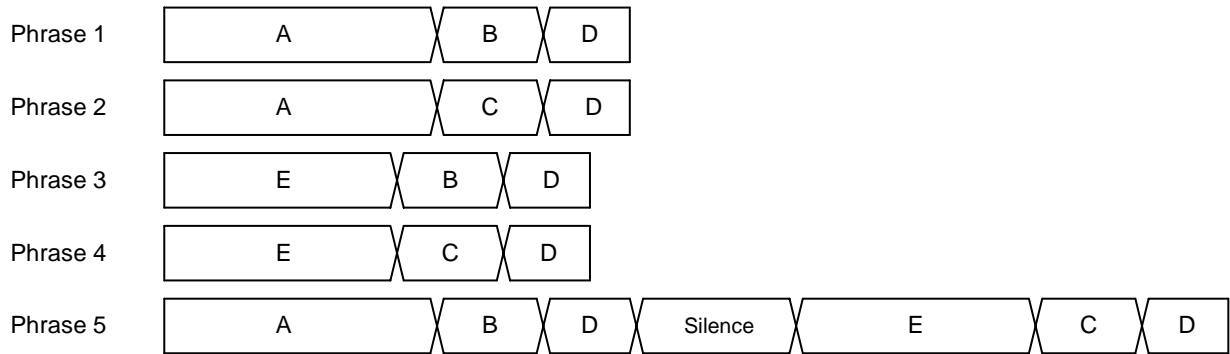
• **Edit ROM Function**

The edit ROM function makes it possible to play back multiple phrases in succession. The following functions are set using the edit ROM function:

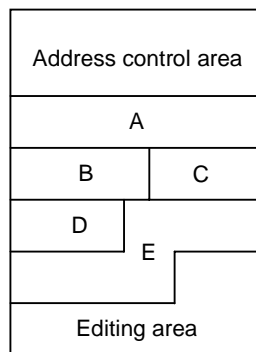
- Continuous playback: There is no limit to the number of times a continuous playback can be specified. It depends on the memory capacity only.
- Silence insertion function: 20 to 1024 ms

Using the edit ROM function enables an effective use of the memory capacity of voice ROM. Below is an example of the ROM configuration in the case of using the edit ROM function.

Example 1 Phrases Using the Edit ROM Function



Example 2 Example of ROM Data Where Contents of Example 1 Are Stored in ROM



• Mixing Function

The ML2282X/ML2286X can perform simultaneous mixing of two channels. It is possible to specify PLAY, STOP, and CVOL for each channel separately.

- Precautions for Waveform Clamp at the Time of Channel Mixing

If channel mixing is done, the possibility of an occurrence of a clamp increases from the mixing calculation point of view. If it is known beforehand that a clamp will occur, then adjust the sound volume of each channel using the VOL command.

• Memory Bank Switching Function

The memory bank switching function enables the the built-in ROM area that is divided into up to four banks to be used. When four banks are used, the maximum number of phrases per bank is 1024 so that up to 4096 phrases can be played back.

Using this function, multiple ROM codes can be grouped into one code.

The settings of SEL1 pin and SEL0 pin determines which memory bank is used. To playback phrases, the number of memory banks must be specified in PUP.

When using a memory bank switching function, data must be divided and saved in the specified areas at ROM data creation.

– When the number of memory banks is 1

SEL1	SEL0	ML22825 ML22865	ML22824 ML22864	ML22823 ML22863
0	0	00000h – 1FFFFFFh	00000h – FFFFFFFh	00000h -7FFFFFFh

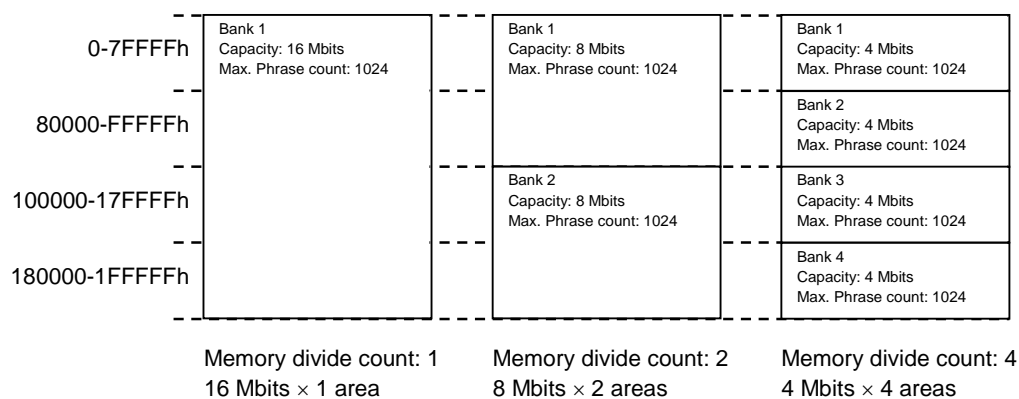
– When the number of memory banks is 2

SEL1	SEL0	ML22825 ML22865	ML22824 ML22864	ML22823 ML22863
0	0	00000h – FFFFFFFh	00000h – 7FFFFFFh	00000h – 3FFFFFFh
0	1	100000h – 1FFFFFFh	80000h – FFFFFFFh	40000h – 7FFFFFFh

– When the number of memory banks is 4

SEL1	SEL0	ML22825 ML22865	ML22824 ML22864	ML22823 ML22863
0	0	00000h – 7FFFFFFh	00000h – 3FFFFFFh	00000h – 1FFFFFFh
0	1	80000h – FFFFFFFh	40000h – 7FFFFFFh	20000h – 3FFFFFFh
1	0	100000h – 17FFFFFFh	80000h – BFFFFFFh	40000h – 5FFFFFFh
1	1	180000h – 1FFFFFFh	C0000h – FFFFFFFh	60000h – 7FFFFFFh

The memory (16 Mbits) in the ML22825 is divided as shown below.



• Description of Command Functions

1. PUP command

• command

0	0	0	0	0	0	S1	S0
---	---	---	---	---	---	----	----

The PUP command is used to shift the ML2282X/ML2286X from a power down state to a command waiting state.

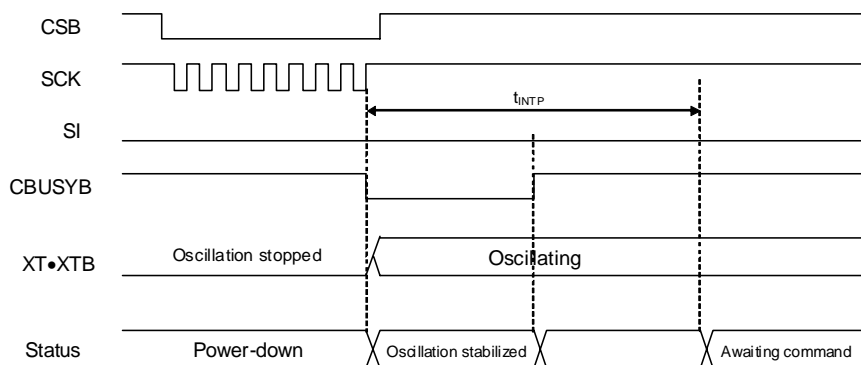
The ML2282X/ML2286X can only accept the PUP command while it is in a power down state. Therefore, in a power-down state, the device will ignore any other command if entered.

The ML2282X/ML2286X enter a power down state under any of the following conditions:

- 1) When power is turned on
- 2) At RESETB input
- 3) When CBUSYB go to a "H" level after inputting the power down command

The relationship between S1/S0 and the memory banks is as follows:

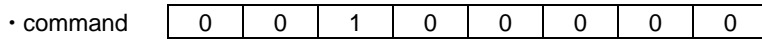
S1	S0	
0	0	Overall memory area is used.
0	1	The internal memory is divided into 2 areas. The 2 memory areas are switched with the SEL0 pin.
1	0	The internal memory is divided into 4 areas. The 4 memory areas are switched with the SEL1 and SEL0 pins.
1	1	Prohibited (The operation is the same as above.)



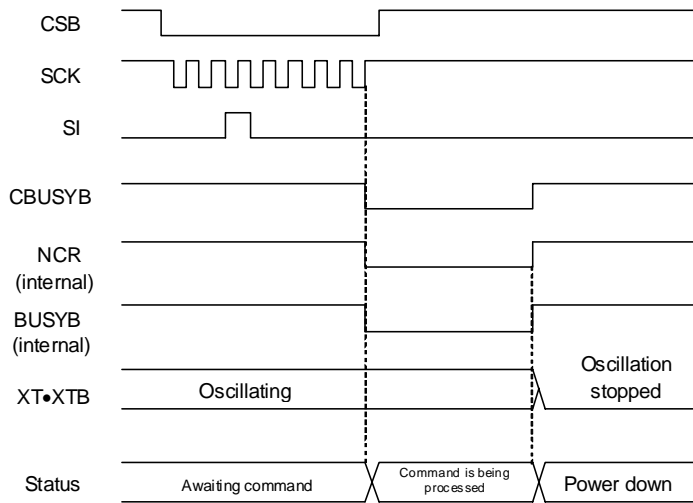
The regulator output starts operating after the PUP command is entered. Any command will be ignored if entered while oscillation is stabilized. However, if a "L" level is input to the RESETB pin, the LSI enters a power down state immediately.

The built-in amplifier is not powered up by the PUP command. It is powered up by the AMODE command.

2. PDWN command



The PDWN command is used to shift the ML2282X/ML2286X from a command waiting state (both NCR and BUSYB are “H”) to a power down state. However, since every setting will be retained even after entering a power down state, no initial setting is required after power-up. This command is invalid during playback. To resume playback after the ML2282X/ML2286X has shifted to a power down state, first input the PUP command and then input the AMODE and the PLAY command.



The regulator and the speaker amplifier stop operation after a lapse of command processing time after the PDWN command is input. At this time, the SPM output of the speaker amplifier goes into a Hi-Z state to prevent generation of pop noise.

Initial status at reset input and status during power down

The status of each output pin is as follows:

Analog output pin	State
V _{DDL}	GND
V _{DDR}	GND
SG	GND
SPM	HiZ
SPP	GND

3. RDSTAT command

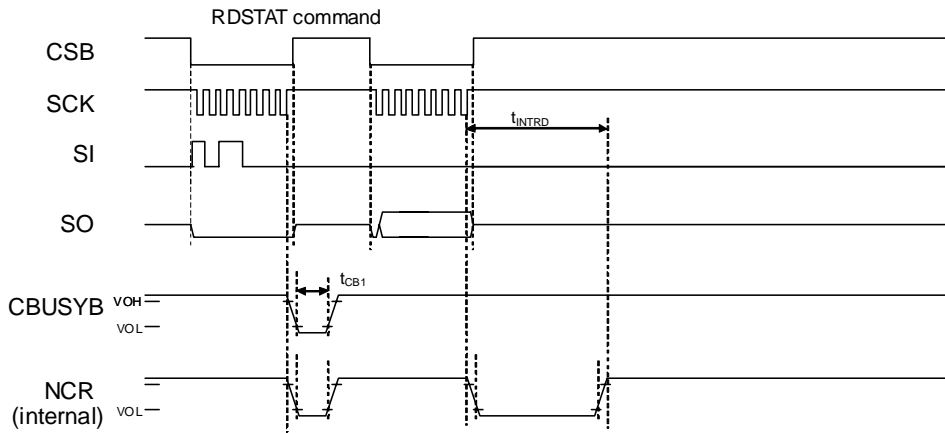
• command

1	0	1	1	0	0	0	0
---	---	---	---	---	---	---	---

The RDSTAT command is used to read the NCR and BUSYB signals that indicate the status of internal operation. The NCR signal outputs a “L” level while this LSI is performing command processing and goes to a “H” level when the LSI enters a command waiting state. The BUSYB signal outputs a “L” level during voice playback.

The table below shows the contents of each data output at a status read.

	Output status signal
MSB	—
7SB	—
6SB	Channel 2 BUSY output (BUSYB1)
5SB	Channel 1 BUSY output (BUSYB0)
4SB	—
3SB	—
2SB	Channel 2 NCR output (NCR1)
LSB	Channel 1 NCR output (NCR0)



4. AMODE command

• command	0	0	0	0	0	1	0	0	1st byte
	FAD	DAG1	DAG0	AIG1	AIG0	DAEN	SPEN	PUP	2nd byte

The AMODE command is used to configure various settings for power-up operation and the analog section. This command is ignored in a power-down state, during transition to a power-up state, or during transition to a power-down state.

The detailed command settings are shown below.

Each setting is initialized upon reset release or power-up.

The FAD bit specifies whether to perform fade-out processing when the STOP command is input. If the bit is set to “1” (Yes), fade-out processing is performed during a period of approx. 3 ms after the STOP command is input. The BUSYB signal goes to a “H” level after fade-out processing.

FAD	Fade-out processing
0	No (initial value)
1	Yes

The DAG1–0 bits are used to set the gain of the internal DAC signal. The AIG1–0 bits are used to set the gain of an analog signal from the AIN pin.

DAG1	DAG0	Volume
0	0	Input OFF
0	1	Input ON (–6 dB)
1	0	Input ON (0 dB) (initial value)
1	1	Setting prohibited (input ON (0 dB))

AIG1	AIG0	Volume
0	0	Input OFF (initial value)
0	1	Input ON (–6 dB)
1	0	Input ON (0 dB)
1	1	Setting prohibited (input ON (0 dB))

The DAEN bit takes power-up and power-down control of the DAC section.

DAEN	Status of the DAC section
0	Power-down state (initial value)
1	Power-up state

The SPEN bit takes power-up and power-down control of the speaker section. When the SPEN bit = “0”, the SPP pin is configured as a LINE output.

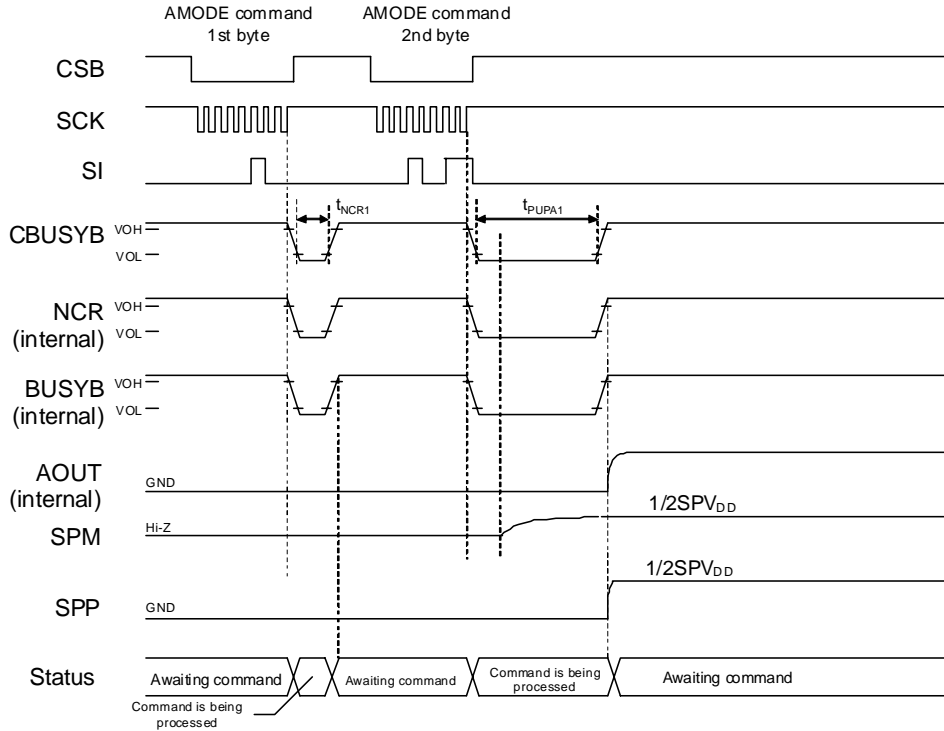
SPEN	Status of the speaker section
0	Power-down state (initial value)
1	Power-up state

The PUP bit specifies whether to suppress generation of “pop” noise.

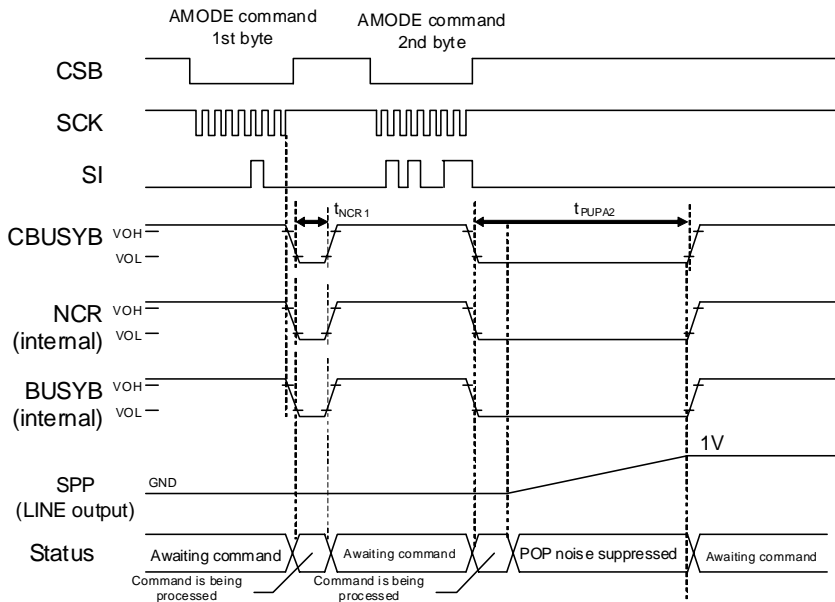
- When the bit is set to “0” (No), if the DAEN bit is “1”, the signal level of the internal amplifier rises from the GND level to the SG level, at which time the speaker amplifier enters a power-up state. If the SPEN bit is “1”, the speaker amplifier enters a power-up state in about 2 ms. If DAEN is “0”, the signal level of the LINE output changes from the SG level to the GND level, at which time the speaker amplifier enters a power-down state. If SPEN is “0”, the speaker amplifier enters a power-down state in about 2 ms.
- When the PUP bit is set to “1” (Yes), if the DAEN bit is “1”, the LINE output goes into a standby state in about 66 ms and then the signal level of the LINE output goes to the SG level, at which time the speaker amplifier enters a power-up state. If the SPEN bit is “1”, the speaker amplifier enters a power-up state in about 66 ms. If the DAEN bit is “0”, the LINE output goes into a standby state in about 66 ms and then the signal level of the LINE output goes to the GND level, at which time the speaker amplifier enters a power-down state. If the SPEN bit is “0”, the speaker amplifier enters a power-down state in about 66 ms.

PUP	Pop noise suppression
0	No (initial value)
1	Yes

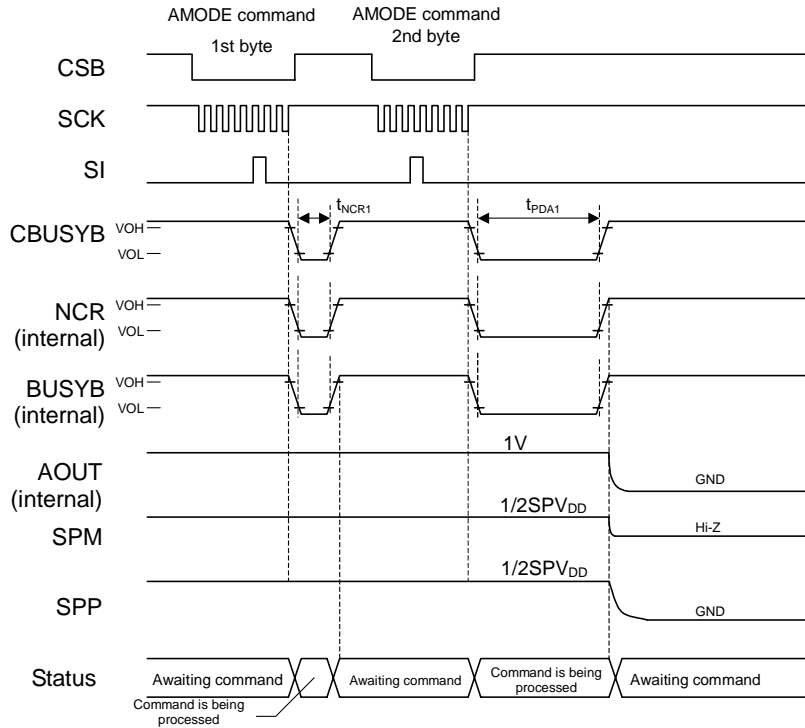
- When PUP bit = “0”, DAEN and SPEN bits = “0” → “1”



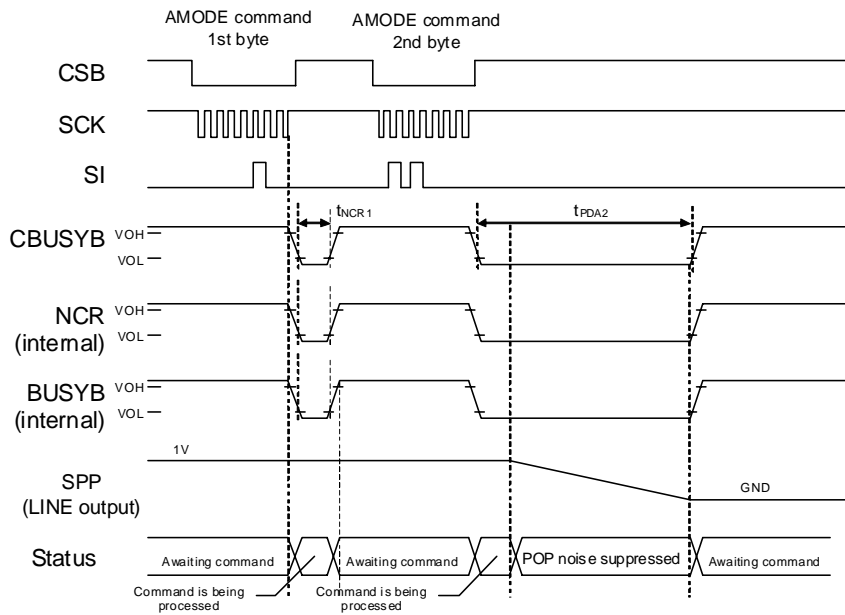
- When PUP bit = “1”, DAEN and SPEN bits = “0” → “1”



- When PUP bit = “0”, DAEN and SPEN bits = “1” → “0”



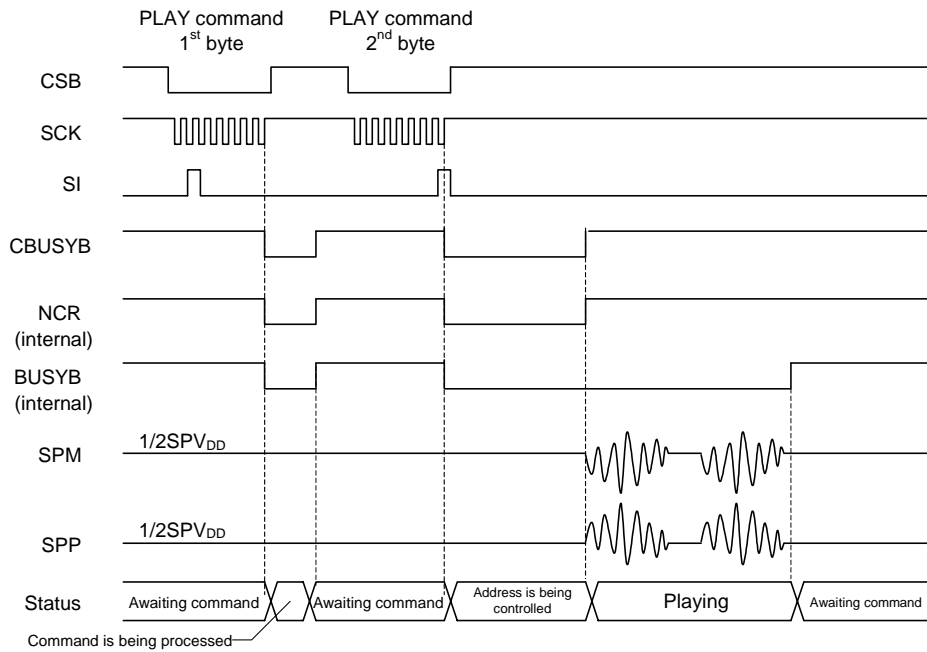
- When PUP bit = “1”, DAEN and SPEN bits = “1” → “0” (Applies only when SPEN = “0”)



5. PLAY command

· command	0	1	0	0	F9	F8	0	CH	1st byte
	F7	F6	F5	F4	F3	F2	F1	F0	2nd byte

The PLAY command is a 2-byte instruction command. This command can be input to each channel when the NCR signal is at the “H” level. The channel to be played back is specified by the by the CH bit. For the phrase to be played back (F9-F0), set the phrase address at the speech data creation. The figure below shows the timing of phrase (F9 to F0 = 01H) playback.



When the 1st byte of the PLAY command is input, the device enters a state awaiting input of the 2nd byte of the PLAY command after a lapse of command processing time. When the 2nd byte of PLAY command is input, after a lapse of command processing time, the device starts reading from the ROM the address information of the phrase to be played. Thereafter, playback operation starts, the playback is performed up to the specified ROM address, and then the playback terminates automatically.

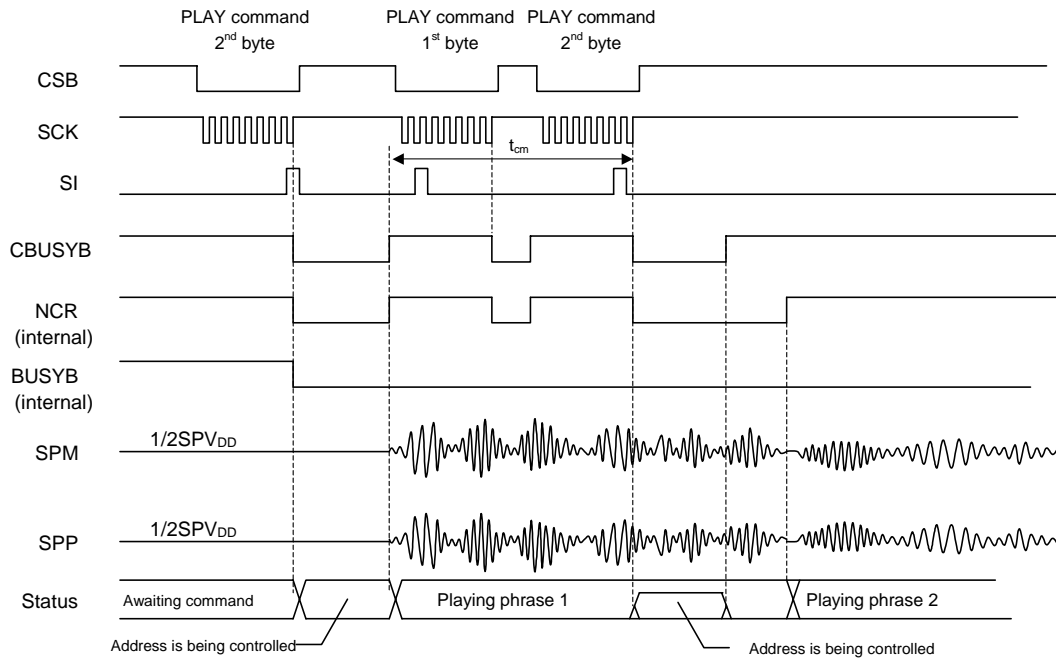
The NCR1 signal is at a “L” level during address control, and goes “H” when the address control is finished. When this NCR signal goes “H”, then it is possible to input the PLAY command for the next playback phrase. During address control, the BUSYB signal is at a “L” level during playback and goes “H” when playback is finished. Whether the playback is going on can be known by the BUSYB signal.

- Channel settings

CH	Channel
0	Channel 1
1	Channel 2

PLAY Command Input Timing for Continuous Playback

The diagram below shows the PLAY command input timing in cases where one phrase is played and then the next phrase is played in succession.



As shown in the diagram above, if continuous playback is carried out, input the PLAY command for the second phrase within 10 ms (t_{cm}) after NCR goes "H". This will make it possible to start playing the second phrase immediately after the playback of the first phrase finishes. Phrases can thus be played continuously without inserting silence between phrases.

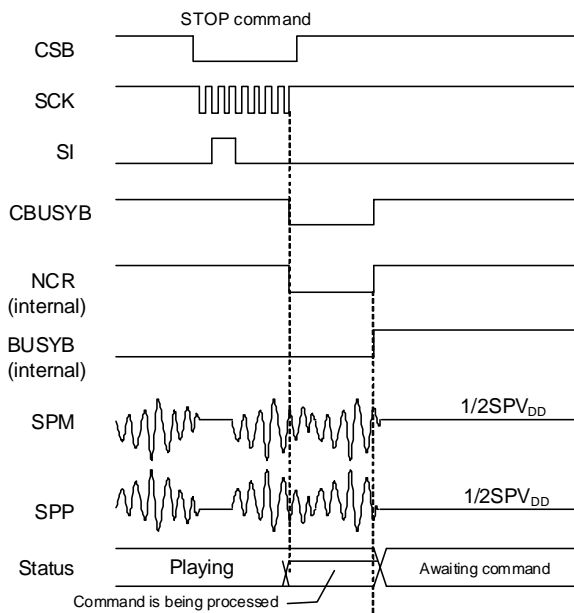
6. STOP command

• command

0	1	1	0	0	0	CH1	CH0
---	---	---	---	---	---	-----	-----

The STOP command is used to stop playback. If speech synthesis processing stops, the NCR and BUSYB signals go to a “H” level. Setting the CH0 or CH1 bit to “H” stops playback on the corresponding channel. Although it is possible to input the STOP command regardless of the status of NCR during playback, a prescribed command interval time needs taking. See “AC Characteristics”.

Note that the STOP command will be ignored if entered during power down or during a transition to a power-up or power-down state.



- Channel settings

	Channel
CH0	Channel 1
CH1	Channel 2

The STOP command allows simultaneous specification of multiple channels.

When a voice playback command (PLAY/START/MUON command) is inputted on the same channel after the STOP command, Please input after confirming completion (NCRn=H, BUSYBn=H) of voice playback stop processing by the RDSTAT command or confirming completion of command processing of the STOP command (after waiting for 12ms from CBUSYB=H).

The PLAY/START/ MUON commands is ignored during voice playback stop processing.

7. FADR command

• command	0	0	1	1	F9	F8	0	CH	1st byte
	F7	F6	F5	F4	F3	F2	F1	F0	2nd byte

The FADR command is used to specify a phrase to be played. A playback channel and phrase are set by this command.

After a playback phrase of each channel is specified, use the START command to start playback. The channel to be played back is specified by the CH bit.

Since it is possible to specify a playback phrase (F9 to F0) at the time of creating a ROM that stores voice data, specify the phrase that was specified when the ROM was created.

The setting values of the FADR command are initialized at power-down.

- Channel settings

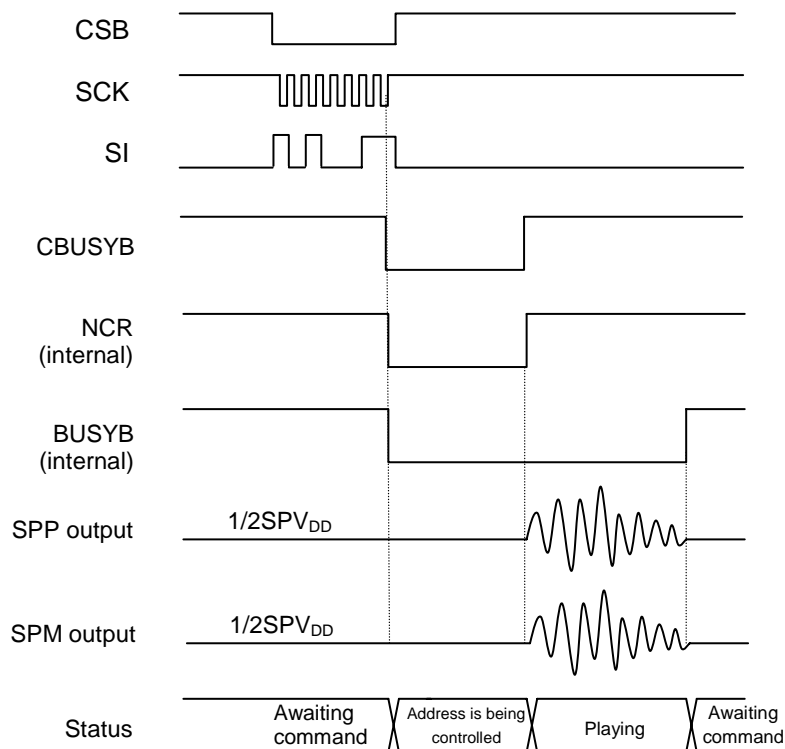
CH	Channel
0	Channel 1
1	Channel 2

8. START command

• command	0	1	0	1	0	0	CH1	CH0
-----------	---	---	---	---	---	---	-----	-----

The START command starts playback of the channel specified. It is necessary to specify a playback phrase using the FADR command before inputting the START command. Use the START command when starting playback on multiple channels simultaneously. Setting the CH0 or CH1 bit to “1” starts playback on the corresponding channel.

The figure below shows the timing when starting playback on 1 channel and 2 channel simultaneously.



- Channel settings

	Channel
CH 0	Channel 1
CH 1	Channel 2

9. MUON command

· command	0	1	1	1	0	0	CH1	CH0	1st byte
	M7	M6	M5	M4	M3	M2	M1	M0	2nd byte

The MUON command is a 2-byte command. This command is used to insert a silence between two playback phrases. The MUON command can be input when the NCR signal is at a “H” level.

Set the silence time length after inputting this command. The MUON command can specify multiple channels simultaneously. Setting the CH0 or CH1 to “H” playbacks silence on the corresponding channel.

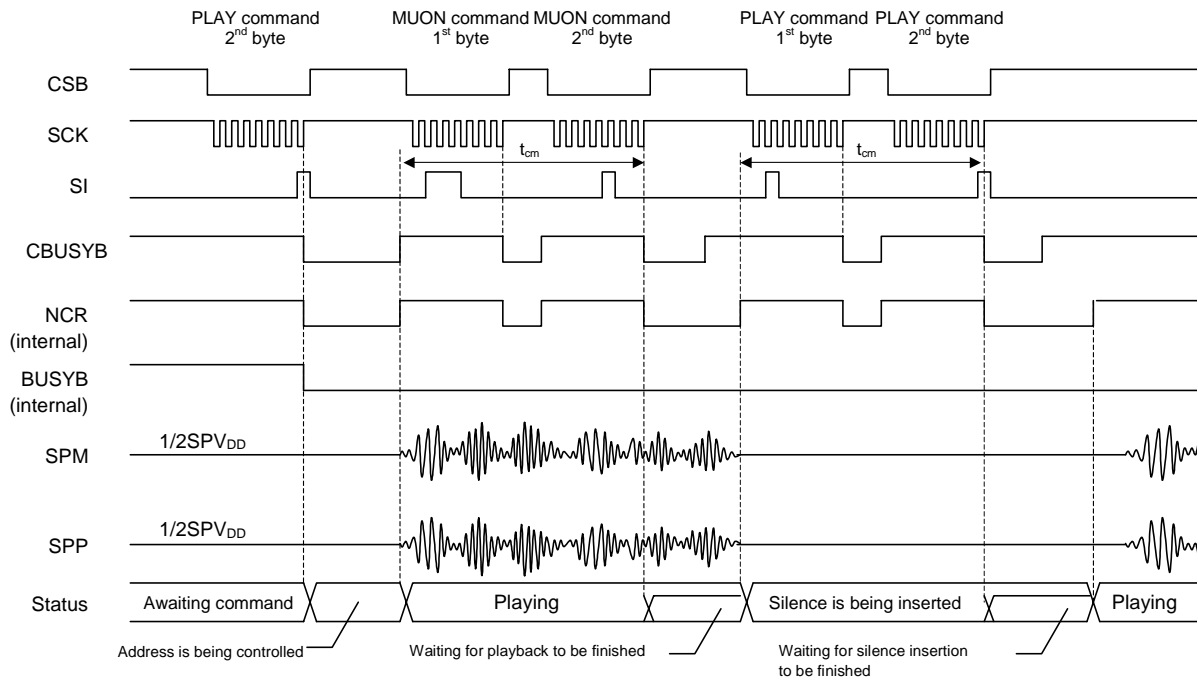
As the silence length (M7 to M0), a value between 20 ms and 1024 ms can be set at 4 ms intervals (252 steps in total).

The equation to set the silence time length is shown below.

The silence length (M7 to M0) must be set to 04h or higher.

$$t_{\text{mu}} = (2^7 \times (M7) + 2^6 \times (M6) + 2^5 \times (M5) + 2^4 \times (M4) + 2^3 \times (M3) + 2^2 \times (M2) + 2^1 \times (M1) + 2^0 \times (M0) + 1) \times 4\text{ms}$$

The figure below shows the timing of inserting a silence of 20 ms between the repetitions of a phrase of (F7–F0) = 01h.



When the PLAY command is input, the address control over phrase 1 ends, the phrase playback starts, and the CBUSYB and NCR signals go to a “H” level. Input the MUON command after this CBUSYB signal changes to a “H” level. After the MUON command input, the NCR signal remains “L” until the end of phrase 1 playback, and the device enters a state waiting for the phrase 1 playback to terminate.

When the phrase 1 playback is terminated, the silence playback starts and the NCR1 signal goes to a “H” level. After this NCR signal has changed to a “H” level, re-input the PLAY command in order to play phrase 1.

After the PLAY command input, the NCR signal once again goes to a “L” level and the device enters a state waiting for the end of silence playback.

When the silence playback is terminated and then the phrase 1 playback starts, the NCR signal goes “H”, and the device enters a state where it is possible to input the next PLAY or MUON command.

The BUSYB signal remains “L” until the end of a series of playback.

10. SLOOP command

• command

1	0	0	0	0	0	0	CH1	CH0
---	---	---	---	---	---	---	-----	-----

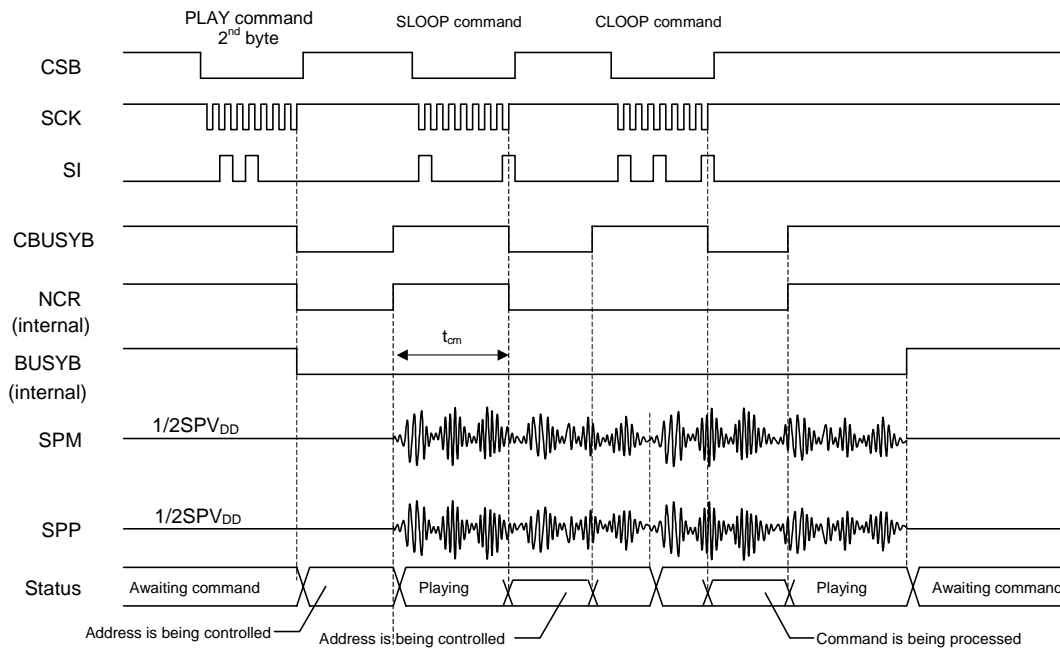
The SLOOP command is used to set repeat playback mode. The SLOOP command can specify multiple channels simultaneously. Setting the CH0 or CH1 to “H” playbacks the corresponding channel repeatedly. To release repeat playback mode, use the CLOOP command.

Since the SLOOP command is only valid during playback, be sure to input the SLOOP command while the NCR signal is at a “H” level after the PLAY command is input. The NCR signal remains “L” during repeat playback mode.

Once repeat playback mode is set, the current phrase is repeatedly played until the repeat playback setting is released by the SLOOP command or until playback is stopped by the STOP command. In the case of a phrase that was edited using the edit function, the edited phrase is repeatedly played.

Repeat playback mode is released if playback is stopped by the STOP command; therefore, if desired to repeat playback after the release of repeat playback mode, input the SLOOP command once again.

Following shows the SLOOP command input timing.



Effective Range of SLOOP Command Input

After the PLAY command is input, input the SLOOP command within 10 ms (t_{cm}) after NCR goes “H”. This will enable the SLOOP command, so that repeat playback will be carried out.

- Channel settings

	Channel
CH 0	Channel 1
CH 1	Channel 2

11. CLOOP command

• command

1	0	0	1	0	0	CH1	CH0
---	---	---	---	---	---	-----	-----

The CLOOP command releases repeat playback mode. The CLOOP command can specify multiple channels simultaneously. Setting the CH0 or CH1 to “H” releases playback on the corresponding channel repeatedly. When repeat playback mode is released, the NCR signal goes “H”.

It is possible to input the CLOOP command regardless of the status of the NCR signal during playback, but a prescribed command interval needs taking.

- Channel settings

	Channel
CH 0	Channel 1
CH 1	Channel 2

12. CVOL command

• command	1	0	1	0	0	0	CH1	CH0	1st byte
	0	0	0	CV4	CV3	CV2	CV1	CV0	2nd byte

The CVOL command is a 2-byte command. It is used to adjust the playback volume of each channel. It is possible to input the VOL command regardless of the status of the NCR signal. Note that the CVOL command is ignored if entered during power down or during a transition to a power-up or power-down state.

The CVOL command can set each channel. The CVOL command can specify multiple channels simultaneously. Setting the CH0 or CH1 bit to "H" sets the playback volume on the corresponding channel(s). The command enables 32-level adjustment of volume, as shown in the table below. The initial value after reset release is set to 0 dB. After reset release or during power-up, the value set by the VOL command is initialized.

CV4	CV3	CV2	CV1	CV0	Volume
0	0	0	0	0	0 dB (initial value)
0	0	0	0	1	-0.28
0	0	0	1	0	-0.58
0	0	0	1	1	-0.88
0	0	1	0	0	-1.20
0	0	1	0	1	-1.53
0	0	1	1	0	-1.87
0	0	1	1	1	-2.22
0	1	0	0	0	-2.59
0	1	0	0	1	-2.98
0	1	0	1	0	-3.38
0	1	0	1	1	-3.81
0	1	1	0	0	-4.25
0	1	1	0	1	-4.72
0	1	1	1	0	-5.22
0	1	1	1	1	-5.74
1	0	0	0	0	-6.31
1	0	0	0	1	-6.90
1	0	0	1	0	-7.55
1	0	0	1	1	-8.24
1	0	1	0	0	-9.00
1	0	1	0	1	-9.83
1	0	1	1	0	-10.74
1	0	1	1	1	-11.77
1	1	0	0	0	-12.93
1	1	0	0	1	-14.26
1	1	0	1	0	-15.85
1	1	0	1	1	-17.79
1	1	1	0	0	-20.28
1	1	1	0	1	-23.81
1	1	1	1	0	-29.83
1	1	1	1	1	OFF

- Channel settings

	Channel
CH 0	Channel 1
CH 1	Channel 2

13. AVOL command

• command	0	0	0	0	1	0	0	0	1st byte
	0	0	AV5	AV4	AV3	AV2	AV1	AV0	2nd byte

The AVOL command is a 2-byte command. It is used to adjust the playback volume. It is possible to input the AVOL command regardless of the status of the NCR signal. The AVOL command is ignored if entered during power down or during a transition to a power-up or power-down state.

The command enables 50-level adjustment of volume, as shown in the table below. The initial value after reset release is set to 0 dB. When the STOP command is input, the value set by the AVOL command is retained. When powered down, the value set by the AVOL command is initialized.

AV5-0	Volume (dB)	AV5-0	Volume (dB)
3F	+16.0	1F	-4.0
3E	+15.5	1E	-5.0
3D	+15.0	1D	-6.0
3C	+14.5	1C	-7.0
3B	+14.0	1B	-8.0
3A	+13.5	1A	-9.0
39	+13.0	19	-10.0
38	+12.5	18	-12.0
37	+12.0	17	-14.0
36	+11.5	16	-16.0
35	+11.0	15	-18.0
34	+10.5	14	-20.0
33	+10.0	13	-22.0
32	+9.5	12	-24.0
31	+9.0	11	-26.0
30	+8.5	10	-28.0
2F	+8.0	0F	-30.0
2E	+7.5	0E	OFF
2D	+7.0	0D	OFF
2C	+6.5	0C	OFF
2B	+6.0	0B	OFF
2A	+5.5	0A	OFF
29	+5.0	09	OFF
28	+4.5	08	OFF
27	+4.0	07	OFF
26	+3.0	06	OFF
25	+2.0	05	OFF
24	+1.0	04	OFF
23	0.0 (initial value)	03	OFF
22	-1.0	02	OFF
21	-2.0	01	OFF
20	-3.0	00	OFF

TERMINATION OF THE SG PIN

The SG pin is the signal ground pin for the built-in speaker amplifier. Connect a capacitor between this pin and the analog ground so that pin will not carry noise.

The recommended capacitance value is shown below; however, it is recommended that the user determine the capacitance value after evaluation.

Always start playback after each output voltage is stabilized.

Pin	Recommended capacitance value	Remarks
SG	0.1 μ F \pm 20%	The larger the connection capacitance, the longer the speaker amplifier output pin (SPM and SPP) voltage stabilization time.

TERMINATION OF THE V_{DDL} AND V_{DDR} PINS

The V_{DDL} pin is the power supply pin for the internal circuits and the V_{DDL} pin is the power supply pin for the P2ROM. Connect a capacitor between this pin and the ground in order to prevent noise generation and power fluctuation.

The recommended capacitance value is shown below; however, it is recommended that the user determine the capacitance value after evaluation.

Always start the next operation after each output voltage is stabilized.

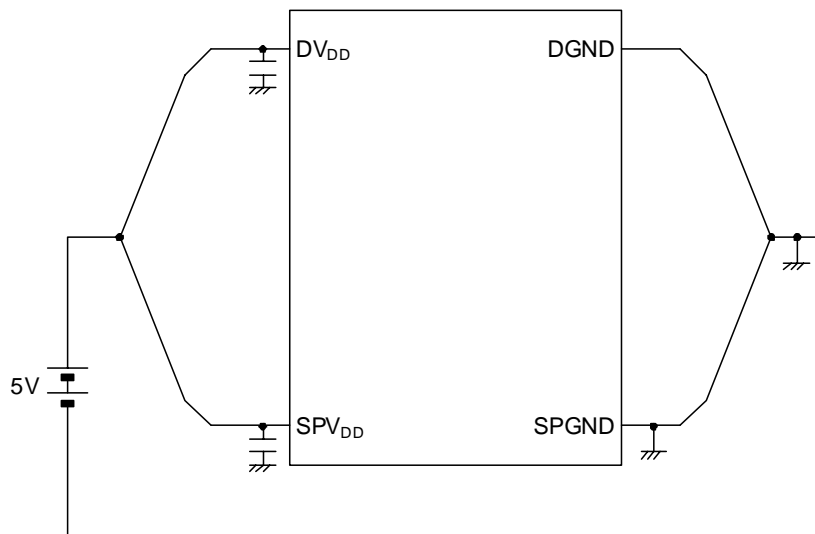
Pin	Recommended capacitance value	Remarks
V _{DDL} , V _{DDR}	1.0 μ F \pm 20%	The larger the connection capacitance, the longer the settling time.

Power Supply Wiring

The power supplies of this LSI are divided into the following two:

- Digital power supply (DV_{DD})
- Speaker amplifier power supply (SPV_{DD})

As shown in the figure below, supply DV_{DD} and SPV_{DD} from the same power supply, and separate them into analog and digital power supplies in the wiring.



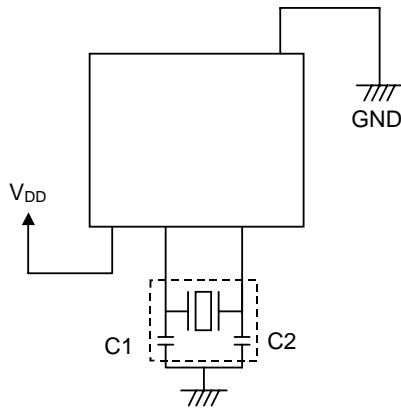
RECOMMENDED CERAMIC OSCILLATION

The optimal load capacities when connecting ceramic resonators from KYOCERA CORPORATION, TDK CORPORATION, and MURATA MFV., are shown below for reference.

KYOCERA Corporation

Freq [Hz]	Type	Optimal load capacity					
		C1 [pF]	C2 [pF]	Rf [Ohm]	Rd [Ohm]	Supply voltage Range [V]	Operating Temperature Range [°C]
4.096M	PBRC4.096MR50X000	15(internal)		---	--	2.7 to3.3 4.5 to5.5	-40 to +85

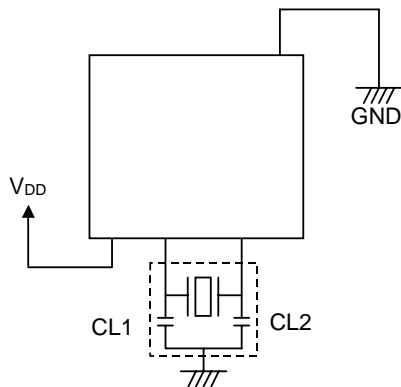
Circuit diagram



TDK Corporation

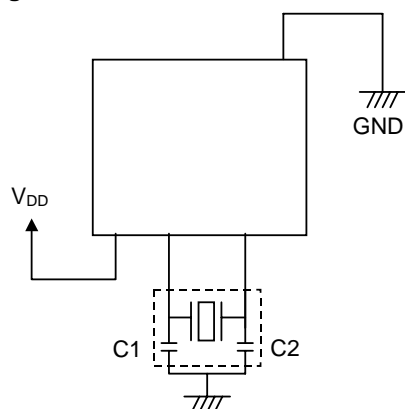
Freq [Hz]	Type	Optimal load capacity					
		C1 [pF]	CL2 [pF]	Rf [Ohm]	C1 [pF]	Supply voltage Range [V]	Operating Temperature Range [°C]
4.000M	FCR4.0MXC5	30 (internal)		---	---	2.7 to3.6	-40 to +85
	FCR4.0MXC5					4.5 to5.5	
4.096M	FCR4.09MXC5	30 (internal)		---	---	2.7 to3.6	-40 to +85
	FCR4.09MXC5					4.5 to5.5	

Circuit diagram

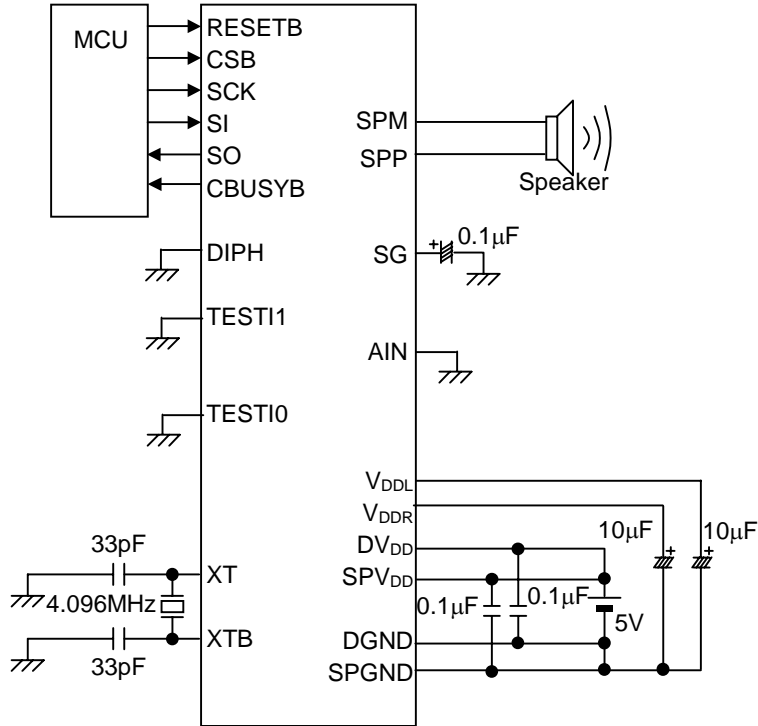


MURATA Corporation

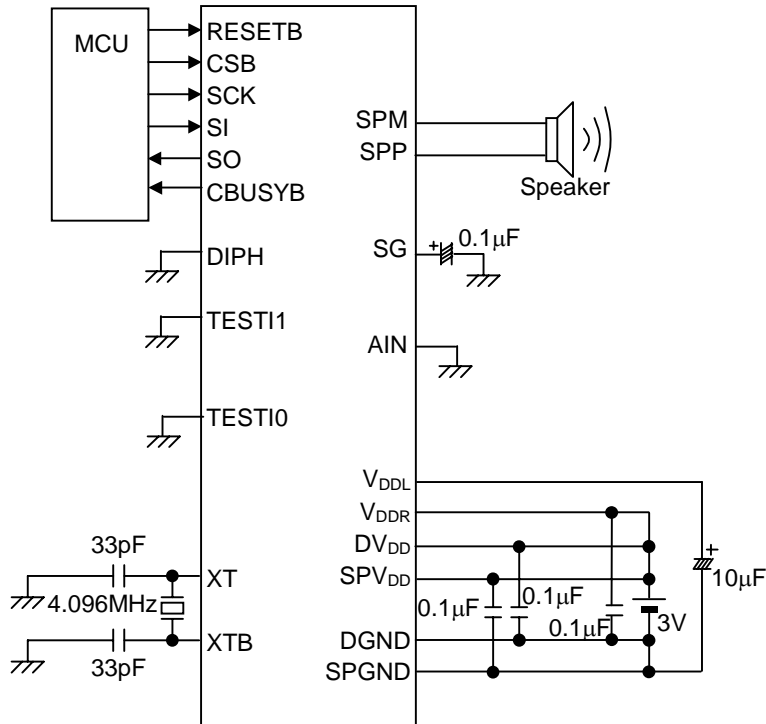
Freq [Hz]	Type		Optimal load capacity					Operating Temperature Range [°C]
			C1 [pF]	C2 [pF]	Rf [Ohm]	Rd [Ohm]	Supply voltage Range [V]	
4.000M	SMD	CSTCR4M00G55-R0	39 (Built-in)		---	0	-40 to +85*	2.7 to 3.6
	Leaded	CSTLS4M00G56-B0	47 (Built-in)					
	SMD	CSTCR4M00G55-R0	39 (Built-in)					4.5 to 5.5
	Leaded	CSTLS4M00G56-B0	47 (Built-in)					
4.096M	SMD	CSTCR4M09G55-R0	39 (Built-in)		---	0	-40 to +85*	2.7 to 3.6
	Leaded	CSTLS4M09G56-B0	47 (Built-in)					
	SMD	CSTCR4M09G55-R0	39 (Built-in)					4.5 to 5.5
	Leaded	CSTLS 4M09G56-B0	47 (Built-in)					

Circuit diagram

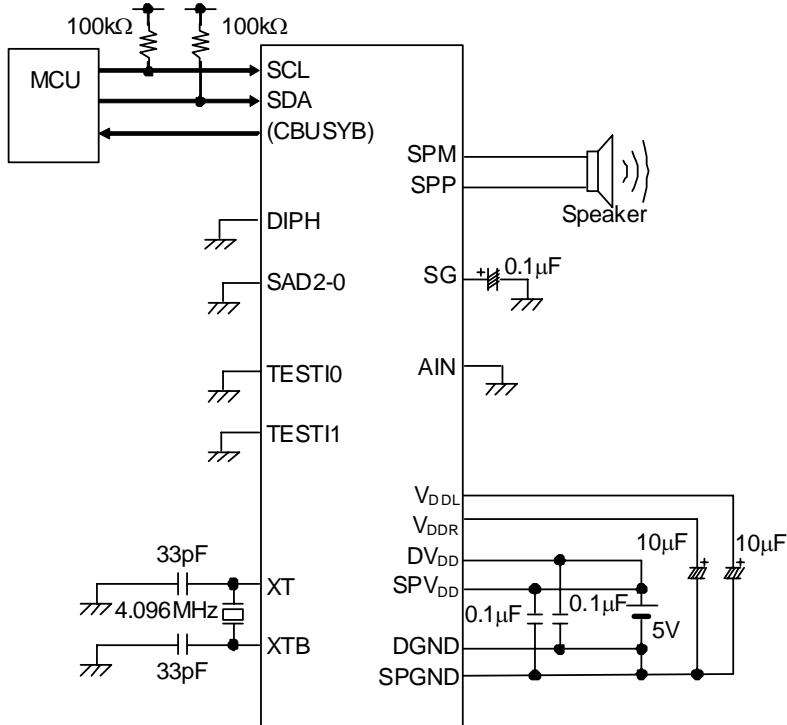
APPLICATION CIRCUIT (ML2282X: DV_{DD} = SPV_{DD} = 5V)



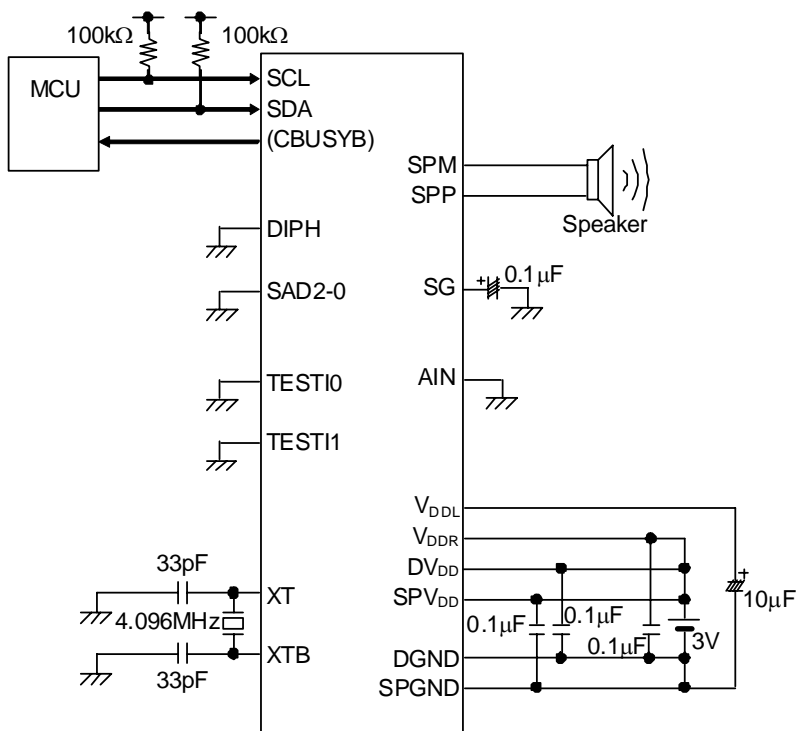
APPLICATION CIRCUIT (ML2282X: DV_{DD} = SPV_{DD} = 3V)



APPLICATION CIRCUIT (ML2286X: DV_{DD}=SPV_{DD}=5V)

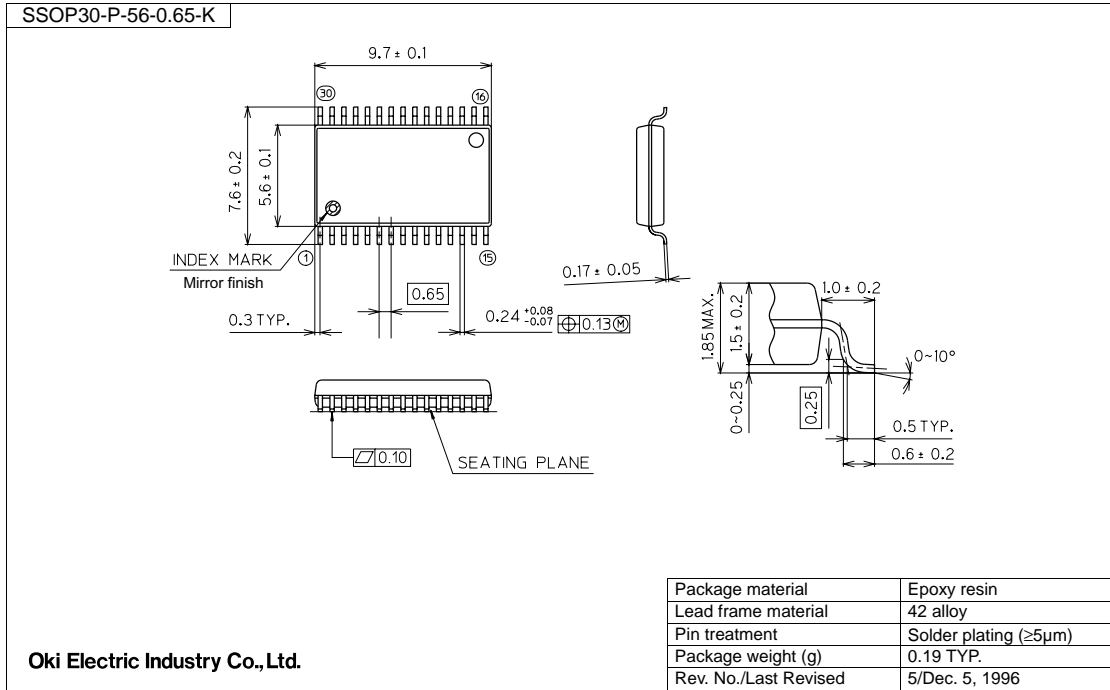


APPLICATION CIRCUIT (ML2286X: DV_{DD}=SPV_{DD}=3V)



PACKAGE DIMENSIONS

(Unit: mm)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact OKI's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL2282XFULL-01	Dec. 17, 2007	–	–	Preliminary edition 1
FEDL228XXFULL-01	Apr. 18, 2008	–	–	Final edition 1
FEDL228XXFULL-02	May. 29, 2008	–	–	Final edition 2

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